DATA TRANSLATION

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DT9800 Series User's Manual

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Radio and Television Interference

This equipment has been tested and found to comply with CISPR EN55022 Class A, and EN50082-1 (CE) requirements and also with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

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Note: This product was verified to meet FCC requirements under test conditions that included use of shielded cables and connectors between system components. It is important that you use shielded cables and connectors to reduce the possibility of causing interference to radio, television, and other electronic devices.

Canadian Department of Communications Statement

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la class A prescrites dans le Règlement sur le brouillage radioélectrique édicté par le Ministère des Communications du Canada.

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About this Manual

This manual describes the features of the DT9800 Series function modules, the capabilities of the DT9800 Series Device Driver, and how to program the DT9800 Series function modules using DT-Open Layers™ software. Calibration and troubleshooting information is also provided.

Intended Audience

This document is intended for engineers, scientists, technicians, or others responsible for using and/or programming the DT9800 Series function modules for data acquisition operations in Microsoft® Windows® 98, Windows Me (Millennium Edition), Windows 2000, Windows XP, or the Macintosh® (MAC OS 9.0) operating system. It is assumed that you have some familiarity with data acquisition principles and that you understand your application.

What You Should Learn from this Manual

This manual provides detailed information about the features of the DT9800 Series function modules and the capabilities of the DT9800 Series Device Driver. The manual is organized as follows:

- Chapter 1, "Overview," describes the major features of the modules, as well as the supported software and accessories for the modules.
- Chapter 2, "Principles of Operation," describes all of the features of the modules and how to use them in your application.
- Chapter 3, "Supported Device Driver Capabilities," lists the data acquisition subsystems and the associated features accessible using the DT9800 Series Device Driver.

- Chapter 4, "Programming Flowcharts," describes the processes you must follow to program the subsystems on the DT9800 Series module using DT-Open Layers-compliant software.
- Chapter 5, "Calibration," describes how to calibrate the analog I/O circuitry of the modules.
- Chapter 6, "Troubleshooting," provides information that you can use to resolve problems with the modules and the device driver, should they occur.
- Appendix A, "Specifications," lists the specifications of the modules.
- Appendix B, "Connector Pin Assignments," shows the pin assignments for the connectors and the screw terminal assignments for the modules.
- An index completes this manual.

Conventions Used in this Manual

The following conventions are used in this manual:

- Notes provide useful information or information that requires special emphasis, cautions provide information to help you avoid losing data or damaging your equipment, and warnings provide information to help you avoid catastrophic damage to yourself or your equipment.
- Items that you select or type are shown in **bold**.

Related Information

Refer to the following documents for more information on using the DT9800 Series function modules:

- *Benefits of the Universal Serial Bus for Data Acquisition.* This white paper describes why USB is an attractive alternative for data acquisition. It is available on the Data Translation web site (www.datatranslation.com).
- *DT9800 Series Getting Started Manual* (UM-17471). This manual, included on the Data Acquisition OMNI CD™, describes the how to install the DT9800 Series function modules and related software.
- *DT Measure Foundry Getting Started Manual* (UM-19298) and online help. These documents describe how to use DT Measure Foundry™ to build drag-and-drop test and measurement applications for Data Translation® data acquisition devices without programming.
- *DataAcq SDK User's Manual* (UM-18326). For programmers who are developing their own application programs using the Microsoft C compiler, this manual describes how to use the DT-Open Layers DataAcq SDK™ to access the capabilities of Data Translation data acquisition devices.
- *DTx-EZ Getting Started Manual* (UM-15428). This manual describes how to use the ActiveX controls provided in DTx-EZ™ to access the capabilities of Data Translation data acquisition devices in Microsoft Visual Basic® or Visual C++®.
- *DT VPI User Manual* (UM-16150). This manual describes how to use DT VPI™ and the Agilent® VEE™ visual programming language to access the capabilities of Data Translation data acquisition devices.
- *DT-LV Link Getting Started Manual* (UM-15790). This manual describes how to use DT-LV Link™ with the LabVIEW® graphical programming language to access the capabilities of Data Translation data acquisition devices.

- Microsoft Windows 98, Windows Me, Windows 2000, Windows XP, or Macintosh documentation.
- USB web site (http://www.usb.org).
- *Omega Complete Temperature Measurement Handbook and Encyclopedia®*. This document, published by Omega Engineering, provides information on how to linearize voltage values into temperature readings for various thermocouple types.

Where To Get Help

Should you run into problems installing or using a DT9800 Series function module, the Data Translation Technical Support Department is available to provide technical assistance. Refer to Chapter 6 for more information. If you are outside the United States or Canada, call your local distributor, whose number is listed in your Data Translation product handbook.

Overview

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Features

The DT9800 Series is a family of low-cost, multifunction data acquisition modules for the Universal Serial Bus (USB). USB is a new standard for connecting PCs to peripheral devices, such as printers, mice, and modems, and was developed to make more low-cost ports available for the increasing number of these devices.

Most new computers have two USB ports that allow direct connection to USB devices. You can expand the number of USB devices attached to a single USB port by using expansion hubs. DT9800 Series function modules are part of the high-power, bus-powered USB class; therefore, the modules do not require external power, but the expansion hubs do require external power.

DT9800 Series function modules reside outside of the PC and install with a single cable to ease installation. Modules can be “hot swapped” or plugged and unplugged while the PC is on, making them useful for many data acquisition applications.

The DT9800 Series includes the following subseries: DT9800 Standard Series, DT9800-MAC Series, DT9800-EC Series, and DT9800-EC-I Series.

The DT9800-EC Series modules are not isolated; the DT9800 Standard Series, DT9800-MAC Series, and DT9800-EC-I Series modules are isolated. In addition, the DT9800-EC and DT9800-EC-I Series modules support the use of optional backplanes and screw terminal panels that provide signal conditioning and other features. Table 1 lists the function modules in each series and the key features of each.

Table 1: Key Features Among the DT9800 Series

Series	Operating System	Function Modules	# of Analog Inputs	Analog Input Sample Rate	# of Analog Outputs	# of Digital I/O Lines	# of Counter /Timers
DT9800 Standard Series	Windows	DT9801[a]	16 SE/ 8 DI	100 kS/s	0	8 input, 8 output	2
		DT9802[a]	16 SE/ 8 DI	100 kS/s	2	8 input, 8 output	2
		DT9803[b]	16 SE/ 8 DI	100 kS/s	0	8 input, 8 output	2
		DT9804[b]	16 SE/ 8 DI	100 kS/s	2	8 input, 8 output	2
		DT9805[c]	16 SE/ 8 DI/ 7 thermo-couples and 1 CJC	50 kS/s	0	8 input, 8 output	2
		DT9806[c]	16 SE/ 8 DI/ 7 thermo-couples and 1 CJC	50 kS/s	2	8 input, 8 output	2

Table 1: Key Features Among the DT9800 Series (cont.)

Series	Operating System	Function Modules	# of Analog Inputs	Analog Input Sample Rate	# of Analog Outputs	# of Digital I/O Lines	# of Counter /Timers
DT9800-MAC Series	Macintosh	DT9801-MAC[a]	16 SE/ 8 DI	100 kS/s	0	8 input, 8 output	2
		DT9802-MAC[a]	16 SE/ 8 DI	100 kS/s	2	8 input, 8 output	2
		DT9803-MAC[b]	16 SE/ 8 DI	100 kS/s	0	8 input, 8 output	2
		DT9804-MAC[b]	16 SE/ 8 DI	100 kS/s	2	8 input, 8 output	2
DT9800-EC Series[d]	Windows	DT9801-EC[a]	16 SE/ 8 DI[e]	100 kS/s	0	8 input, 8 output	2
		DT9802-EC[a]	16 SE/ 8 DI[e]	100 kS/s	2[f]	8 input, 8 output	2
		DT9803-EC[b]	16 SE/ 8 DI[g]	100 kS/s	0	8 input, 8 output	2
		DT9804-EC[b]	16 SE/ 8 DI[g]	100 kS/s	2[h]	8 input, 8 output	2
DT9800-EC-I Series[d]	Windows	DT9801-EC-I[a]	16 SE/ 8 DI[e]	100 kS/s	0	8 input, 8 output	2
		DT9802-EC-I[a]	16 SE/ 8 DI[e]	100 kS/s	2[f]	8 input, 8 output	2
		DT9803-EC-I[b]	16 SE/ 8 DI[g]	100 kS/s	0	8 input, 8 output	2
		DT9804-EC-I	16 SE/ 8 DI[g]	100 kS/s	2[h]	8 input, 8 output	2

a. The resolution is 12 bits.
b. The resolution is 16 bits.

c. The gains provided on the DT9805 and DT9806 are 1, 10, 100, and 500. All other modules provide gains of 1, 2, 4, and 8.
d. The DT9800-EC Series boards are nonisolated; the DT9800-EC-I Series boards and all other DT9800 Series boards are isolated.
e. The analog input range is 0 to 10 V or ±10 V.
f. The analog output range is 0 to 10 V, 0 to 5 V, ±10 V, or ±5 V.
g. The analog input range is ±10 V.
h. The analog output range is ±10 V.

All DT9800 Series function modules share the following major features:

- USB compatibility;
- Software configurable termination resistance for differential inputs on a channel-by-channel basis.
- Input gains of 1, 2, 4, and 8 for all modules except the DT9805 and DT9806, which support gains of 1, 10, 100, and 500;
- Continuously paced and triggered scan capability;
- A 32-location channel-gain list that supports sampling analog input channels at the same or different gains in sequential or random order;
- Internal and external clock sources for the analog input subsystem;
- Digital TTL triggering for the analog input subsystem;
- One 8-bit digital input port and one 8-bit digital output port; the digital input lines can be included as part of the analog input channel-gain list to correlate the timing of analog and digital events; digital outputs can drive external solid-state relays; and
- One dynamic digital output line;
- Two 16-bit user counter/timers programmable for event counting, frequency measurement, rate generation (continuous pulse output), one-shot, and repetitive-one shot pulse output operations.
- Programmable gate types and pulse output types.

In addition, the DT9805 and DT9806 function modules provide thermocouples and low-level analog input capability. The DT9800 Standard, DT9800-EC, and DT9800-EC-I Series modules also provide software calibration for the analog I/O subsystems.

Supported Software

The following software is available for use with the DT9800 Series modules:

- **DT9800 Series Device Driver** –This software is provided on the Data Acquisition OMNI CD™ (for Windows 98, Windows Me, Windows 2000, and Windows XP) or the DT9800 Series CD-ROM for the Macintosh, and is shipped with the module. The device driver allows you to use a DT9800 Series function module with any of the supported software packages or utilities. Refer to the *DT9800 Series Getting Started Manual* (UM-17471) for more information on loading and configuring the device driver.
- **Quick Data Acq application** –This software is provided on the Data Acquisition OMNI CD (for Windows 98, Windows Me, Windows 2000, and Windows XP) or the DT9800 Series CD-ROM for the Macintosh, and is shipped with the module. The Quick Data Acq application provides a quick way to get up and running using a DT9800 Series function module. Using this application, you can verify key features of the modules, display data on the screen, and save data to disk. Refer to the *DT9800 Series Getting Started Manual* (UM-17471) for more information on using the Quick Data Acq application.
- **Scope application** –This software is shipped with the board on the Data Acquisition OMNI CD. This application emulates three basic instruments: a simple oscilloscope chart recorder, a data logger, and a multi-channel oscilloscope. Using the Scope application, you can monitor data online and capture it to disk. Refer to the online documentation provided on the CD-ROM for more information.
- **Calibration Utility** –This software is provided on the Data Acquisition OMNI CD-ROM (for Windows 98, Windows Me, Windows 2000, and Windows XP). (Currently, this utility is not provided for the Macintosh.) The Calibration Utility allows you to calibrate the analog I/O circuitry of the function modules. Refer to Chapter 5 for more information on this utility.

- **DT Measure Foundry** –An evaluation version of this software is included on the Data Acquisition OMNI CD. DT Measure Foundry is drag-and-drop test and measurement application builder designed to give you top performance with ease-of-use development. Order the full development version of this software package to develop your own application using real hardware.
- **DataAcq SDK** –This software is shipped on the Data Acquisition OMNI CD. Use the Data Acq SDK if you want to use Windows 98, Windows Me, Windows NT 4.0, Windows 2000, or Windows XP to develop your own application software for the DT9800 Series boards using the Microsoft C compiler; the DataAcq SDK complies with the DT-Open Layers standard.
- **DTx-EZ** –Order this optional software package if you want to use ActiveX controls to access the capabilities of the DT9800 Series boards using Microsoft Visual Basic or Visual C++; DTx-EZ complies with the DT-Open Layers standard.
- **DT VPI** –Order this optional software package if you want to use the Aglient VEE visual programming language to access the capabilities of the DT9800 Series boards.
- **DT-LV Link** –Order this optional software package if you want to use the LabVIEW graphical programming language to access the capabilities of the DT9800 Series boards.
- **Testpoint** –Order this optional software package if you want use a drag-and-drop software environment for designing test, measurement, and data acquisition applications.

Refer to the Data Translation data acquisition catalog for information about selecting the right software package for your needs.

Accessories

One EP310 cable is shipped with each DT9800 Series function module. The EP310 is a 2-meter, USB cable that connects the USB connector of the DT9800 Series function module to the USB connector on the host computer. If you want to buy additional USB cables, EP310 is available as an accessory product for the DT9800 Series.

In addition, you can purchase the following optional items from Data Translation for use with the DT9800 Series:

- **EP316** –a 5-meter, USB cable that connects the USB connector of the DT9800 Series function module to the USB connector on the host computer.
- **5B01** –a 16-channel backplane that accepts 5B Series signal conditioning modules.
- **5B08** –an 8-channel backplane that accepts 5B Series signal conditioning modules.
- **PWR-977 power supply** –A 5 V, 3 A power supply for powering the 5B Series backplanes.
- **7BP16-1** –a 16-channel backplane that accepts 7B Series signal conditioning modules.
- **7BP08-1** –an 8-channel backplane that accepts 7B Series signal conditioning modules.
- **7BP04-1** –a 4-channel backplane that accepts 7B Series signal conditioning modules.
- **AC1324** –a screw terminal panel that connects to a DT9800-EC or DT9800-EC-I Series function module to allow access to the analog I/O, dynamic digital output, counter/timer, and power signals.
- **PB16H** –a digital backplane that connects to the DT9800-EC or DT9800-EC-I function module to allow access to the digital I/O signals.

- **STP-EZ** –a screw terminal panel that connects to a DT9800-EC or DT9800-EC-I Series function module to allow access to the digital I/O signals. A 50-pin ribbon cable is provided with the STP-EZ to allow direct connection to a DT9800-EC or DT9800-EC-I Series function module.
- **AC1315** –a 2-foot, 26-pin female to 26-pin female cable that connects a 5B Series backplane to a DT9800-EC or DT9800-EC-I Series function module.
- **AC1393** –a 6-inch, 26-pin male to 25-pin female adapter cable that connects a 7B Series backplane to the AC1315 cable; the AC1315 cable then connects to a DT9800-EC or DT9800-EC-I Series function module.
- **HES14-21 power supply** –A linear ac/dc power supply that provides +24 Vdc for powering 7B Series backplanes.
- **EP035** –a 2.4-meter, 50-pin ribbon cable that connects the PB16H Opto 22 backplane to a DT9800-EC or DT9800-EC-I Series function module.

Principles of Operation

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Figure 1 shows a block diagram of the DT9800 Series function modules. Note that bold entries indicate signals you can access.

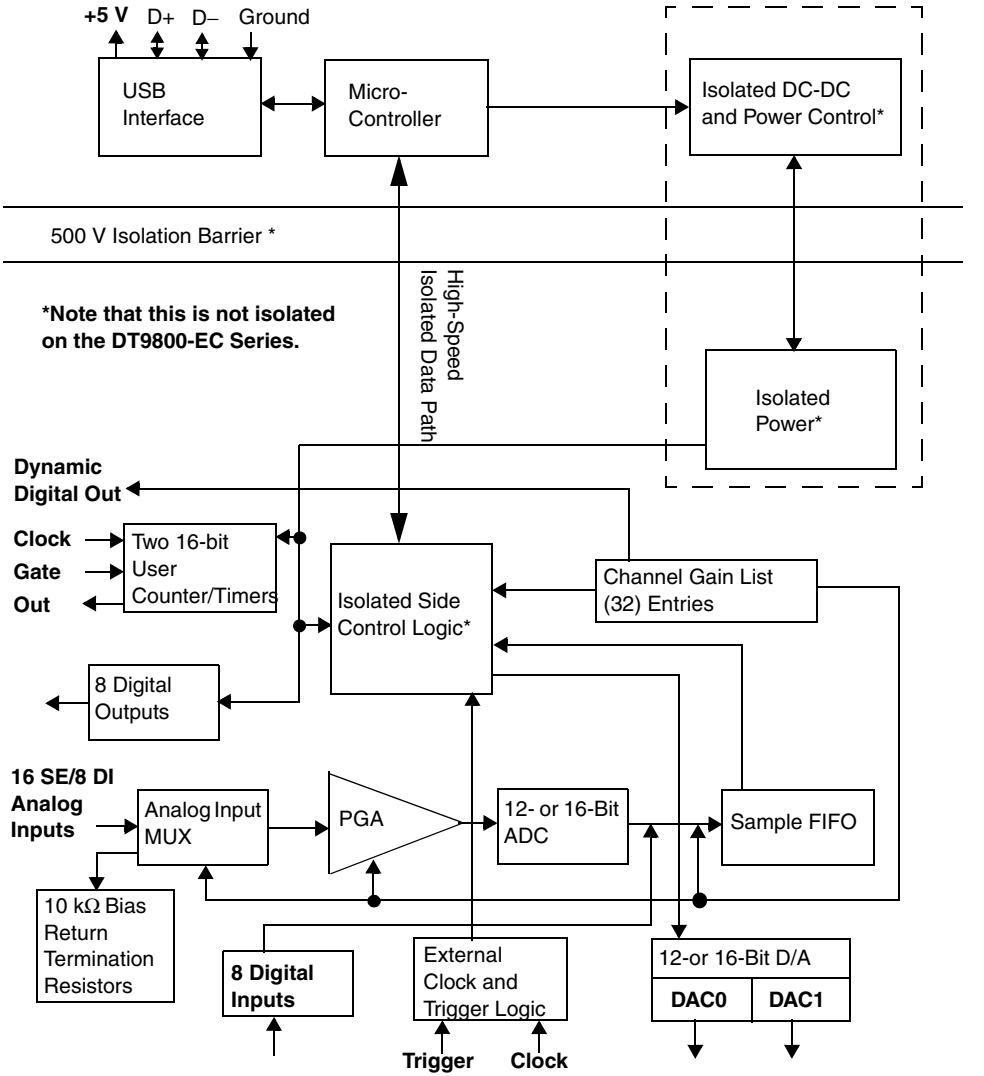


Figure 1: Block Diagram of the DT9800 Series Function Modules

Analog Input Features

This section describes the features of the analog input (A/D) subsystem, including the following:

- Input resolution, described on this page;
- Analog input channels, described on this page;
- Input ranges and gains, described on page 19;
- A/D sample clock sources, described on page 23;
- Analog input conversion modes, described on page 26;
- Triggers, described on page 25;
- Data formats, described on page 33;
- Data transfer, described on page 36; and
- Error conditions, described on page 37.

Input Resolution

Table 2 lists the input resolution of the DT9800 Series function modules. Note that the resolution is fixed; it cannot be programmed in software.

Table 2: Input Resolution

Function Module Series	Module Name	Input Resolution
DT9800 Standard	DT9801 DT9802	12 bit
	DT9803 DT9804 DT9805 DT9806	16 bit

Table 2: Input Resolution (cont.)

Function Module Series	Module Name	Input Resolution
DT9800-MAC Series	DT9801-MAC DT9802-MAC	12 bit
	DT9803-MAC DT9804-MAC	16 bit
DT9800-EC Series	DT9801-EC DT9802-EC	12 bit
	DT9803-EC DT9804-EC	16 bit
DT9800-EC-I Series	DT9801-EC-I DT9802-EC-I	12 bit
	DT9803-EC-I DT9804-EC-I	16 bit

Analog Input Channels

All DT9800 Series function modules support 16 single-ended or pseudo-differential analog input channels or eight differential analog input channels. In addition, the DT9805 and DT9806 function modules provide a cold junction compensation (CJC) circuit on channel 0 at 10 mV/° C. Using the CJC, you can connect seven thermocouple inputs (in differential mode) to the DT9805 or DT9806 module.

You configure the channel type as single-ended or differential through software. Using software, you can also select whether to use 10 kΩ termination resistance between the low side of each differential channel and isolated analog ground. This feature is particularly useful with floating signal sources. Refer to the *DT9800 Series Getting*

Started Manual for more information on wiring to inputs and configuring the driver to use bias return termination resistance.

Note: For pseudo-differential inputs, specify single-ended in software; in this case, how you wire these signals determines the configuration.

The DT9800-EC Series boards do not provide isolated analog ground.

The DT9800 Series function modules can acquire data from a single analog input channel or from a group of analog input channels. Channels are numbered 0 to 15 for single-ended and pseudo-differential inputs, and 0 to 7 for differential inputs. The following subsections describe how to specify the channels.

Specifying a Single Channel

The simplest way to acquire data from a single channel is to specify the channel for a single-value analog input operation using software; refer to page 26 for more information on single-value operations.

You can also specify a single channel using the analog input channel list, described in the next section.

Note: If you want to perform a single-value digital input operation while the A/D subsystem is configured, specify channel 16 (which corresponds to the digital input port) in the A/D single-value operation.

Specifying One or More Channels

You can read data from one or more analog input channels using an analog input channel list. You can group the channels in the list sequentially (starting either with 0 or with any other analog input channel) or randomly. You can also specify a single channel or the same channel more than once in the list.

Using software, specify the channels in the order you want to sample them. You can enter up to 32 entries in the channel list. The channels are read in order (using continuously paced scan mode or triggered scan mode) from the first entry to the last entry in the channel list. Refer to page 26 for more information on the supported conversion modes.

Specifying Digital Input Lines in the Analog Input Channel List

In addition to the analog input channels, the DT9800 Series function modules allow you to read eight digital input lines (Port A, lines 0 to 7) using the analog input channel list. This feature is particularly useful when you want to correlate the timing of analog and digital events.

To read these eight digital input lines, specify channel 16 in the analog input channel list. You can enter channel 16 anywhere in the list and can enter it more than once, if desired.

Note: If channel 16 is the only channel in the channel-gain list, the module can read this channel at the maximum A/D sampling rate.

The digital channel is treated like any other channel in the analog input channel list; therefore, all the clocking, triggering, and conversion modes supported for analog input channels are supported for these digital input lines, if you specify them this way.

Performing Dynamic Digital Output Operations

Using software, you can enable a synchronous dynamic digital output operation for the A/D subsystem. This feature is particularly useful for synchronizing and controlling external equipment.

One dynamic digital output line (0) is provided (screw terminal 46). This line is set to a value of 0 on power up; a reset does not affect the values of the dynamic digital output line. Note that this line is provided in addition to the other eight digital output lines; see page 44 for more information on the digital I/O features.

You specify the value (0 or 1) to write from the dynamic digital output line using a digital channel list. A value of 0 indicates a low-level signal; a value of 1 indicates a high-level signal.

The digital channel list corresponds to the analog input channel list. As each entry in the analog input channel list is read, the corresponding value you specified in the digital channel list is output to the dynamic digital output line.

For example, assume that the analog input channel list contains channels 0, 1, 2, and 3; that dynamic digital output operations are enabled; and that the values in the digital channel list are 1, 0, 0, 1. Figure 2 shows this configuration.

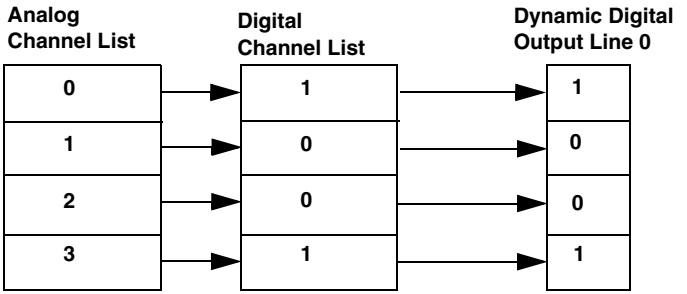


Figure 2: An Example Using Dynamic Digital Outputs

As analog input channel 0 is read, a high-level signal is output to the dynamic digital output line. As analog input channels 1 and 2 are read, a low-level signal is output to the dynamic digital output line. As analog input channel 3 is read, a high-level signal is output to the dynamic digital output line.

On power up, a value of 0 is written to the dynamic digital output line.

Input Ranges and Gains

Table 3 lists the supported gains and effective input range of each DT9800 Series function module.

Table 3: Effective Input Range

Function Module Series	Module Name	Gain	Unipolar Input Range	Bipolar Input Range
DT9800 Standard	DT9801 DT9802	1	0 to 10 V	±10 V
		2	0 to 5 V	±5 V
		4	0 to 2.5 V	±2.5 V
		8	0 to 1.25 V	±1.25 V
	DT9803 DT9804	1	N/A	±10 V
		2	N/A	±5 V
		4	N/A	±2.5 V
		8	N/A	±1.25 V
	DT9805 DT9806	1	N/A	±10 V
		10	N/A	±1 V
		100	N/A	±0.10 V
		500	N/A	±0.020 V

Table 3: Effective Input Range (cont.)

Function Module Series	Module Name	Gain	Unipolar Input Range	Bipolar Input Range
DT9800-MAC Series	DT9801-MAC DT9802-MAC	1	0 to 10 V	±10 V
		2	0 to 5 V	±5 V
		4	0 to 2.5 V	±2.5 V
		8	0 to 1.25 V	±1.25 V
	DT9803-MAC DT9804-MAC	1	N/A	±10 V
		2	N/A	±5 V
		4	N/A	±2.5 V
		8	N/A	±1.25 V
DT9800-EC Series	DT9801-EC DT9802-EC	1	0 to 10 V	±10 V
		2	0 to 5 V	±5 V
		4	0 to 2.5 V	±2.5 V
		8	0 to 1.25 V	±1.25 V
	DT9803-EC DT9804-EC	1	N/A	±10 V
		2	N/A	±5 V
		4	N/A	±2.5 V
		8	N/A	±1.25 V

Table 3: Effective Input Range (cont.)

Function Module Series	Module Name	Gain	Unipolar Input Range	Bipolar Input Range
DT9800-EC-I Series	DT9801-EC-I DT9802-EC-I	1	0 to 10 V	±10 V
		2	0 to 5 V	±5 V
		4	0 to 2.5 V	±2.5 V
		8	0 to 1.25 V	±1.25 V
	DT9803-EC-I DT9804-EC-I	1	N/A	±10 V
		2	N/A	±5 V
		4	N/A	±2.5 V
		8	N/A	±1.25 V

Using software, specify 0 to 10 V for unipolar ranges or –10 V to +10 V for bipolar ranges. Note that you specify the range for the entire analog input subsystem, not the range per channel.

For each channel, choose the gain that has the smallest effective range that includes the signal you want to measure. For example, if you are using a DT9803 and the range of your analog input signal is ±1.05 V, specify a range of –10 V to +10 V for the module and use a gain of 8 for the channel; the effective input range for this channel is then ±1.25 V, which provides the best sampling accuracy for that channel.

The way you specify gain depends on how you specified the channels, as described in the following subsections.

Note: The DT9805 and DT9806 modules support autoranging for single-value operations, where the board determines the appropriate gain for your range rather than you having to specify it. Refer to page 26 for more information on using autoranging.

Specifying the Gain for a Single Channel

The simplest way to specify gain for a single channel is to specify the gain for a single-value analog input operation using software; refer to page 26 for more information on single-value operations.

You can also specify the gain for a single channel using an analog input gain list, described in the next section.

Specifying the Gain for One or More Channels

For DT9800 Series function modules, you can specify the gain for one or more analog input channels using an analog input gain list. Using software, set up the gain list by specifying the gain for each entry in the channel list. (The two lists together are often referred to as the channel-gain list.)

For example, assume the analog input channel list contains three entries: channels 5, 6, and 7; the gain list might look like this: 2, 4, 1, where a gain of 2 corresponds to channel 5, a gain of 4 corresponds to channel 6, and a gain of 1 corresponds to channel 7.

Note: For analog input channel 16 (the eight digital input lines) in the channel list, specify a gain of 1 in the gain list.

A/D Sample Clock Sources

The DT9800 Series function modules allow you to use one of two clock sources for pacing analog input operations in continuous mode:

- The internal A/D sample clock, which uses the 24-bit A/D Counter on the module, or
- An external A/D sample clock, which you can connect to the screw terminal panel.

You use an A/D sample clock to pace the acquisition of each channel in the channel-gain list; this clock is also called the A/D pacer clock.

Note: If you enter digital input channel 16 in the channel-gain list, the A/D sample clock (internal or external) also paces the acquisition of the eight digital input lines.

The following subsections describe the internal and external A/D sample clocks in more detail.

Internal A/D Sample Clock

The internal A/D sample clock uses a 12 MHz time base. Conversions start on the rising edge of the counter output; the output pulse is active low.

Using software, specify the clock source as internal and the clock frequency at which to pace the operation. The minimum frequency supported is 0.75 Hz (0.75 Samples/s); the maximum frequency supported depends on the module type. Table 4 lists the maximum sampling rate of the DT9800 Series function modules.

Table 4: Maximum Sampling Rate

Function Module Series	Module Name	Sampling Rate
DT9800 Standard	DT9801 DT9802 DT9803 DT9804	100 kSamples/s
	DT9805[a] DT9806[a]	50 kSamples/s
DT9800-MAC	DT9801-MAC DT9802-MAC DT9803-MAC DT9804-MAC	100 kSamples/s
DT9800-EC	DT9801-EC DT9802-EC DT9803-EC DT9804-EC	100 kSamples/s
DT9800-EC-I	DT9801-EC-I DT9802-EC-I DT9803-EC-I DT9804-EC-I	100 kSamples/s

a. The maximum rate is 50 kSamples/s for a single channel or a channel scan when the gain is 1 or 10, 10 kSamples/s for a channel scan when the gain is 100, and 2 kSamples/s for a channel scan when the gain is 500.

According to sampling theory (Nyquist Theorem), specify a frequency that is at least twice as fast as the input's highest frequency component. For example, to accurately sample a 20 kHz signal, specify a sampling frequency of at least 40 kHz. Doing so avoids an error condition called *aliasing*, in which high frequency input components erroneously appear as lower frequencies after sampling.

External A/D Sample Clock

An external A/D sample clock is useful when you want to pace acquisitions at rates not available with the internal A/D sample clock or when you want to pace at uneven intervals.

Connect an external A/D sample clock to screw terminal TB25 on the DT9800 Series function module (pin 25 on connector J1). Conversions start on the rising edge of the external A/D sample clock input signal.

Using software, specify the clock source as external. For DT9800 Series function modules, the clock frequency is always equal to the frequency of the external A/D sample clock input signal that you connect to the module through the screw terminal panel.

Triggers

A trigger is an event that occurs based on a specified set of conditions. The DT9800 Series function module supports the following trigger sources:

- **Software trigger** –A software trigger event occurs when you start the analog input operation (the computer issues a write to the module to begin conversions). Using software, specify the trigger source as a software trigger.
- **External trigger** –An external digital trigger event occurs when the DT9800 Series module detects a rising edge on the Ext A/D Trigger input signal connected to screw terminal TB24 on the DT9800 Series module (pin 24 of connector J1). The trigger signal is TTL-compatible. Using software, specify the trigger source as a external digital trigger (external for DataAcq SDK users).

Analog Input Conversion Modes

DT9800 Series function modules support the following conversion modes:

- **Single-value operations** are the simplest to use. Using software, you can either specify the range, gain, and analog input channel, or you can specify the range and analog input channel and have the software determine the best gain for the range (called autoranging). The board acquires the data from the specified channel and returns the data immediately. Data can be returned as both counts and voltage. For a single-value operation, you cannot specify a clock source, trigger source, scan mode, or buffer.

  Single-value operations stop automatically when finished; you cannot stop a single-value operation.

- **Scan mode** takes full advantage of the capabilities of the DT9800 Series function modules. In a scan, you can specify a channel-gain list, clock source, trigger source, scan mode, buffer, and buffer wrap mode using software. Two scan modes are supported: continuously paced scan mode and triggered scan mode (often called burst mode). These modes are described in the following subsections.

  Using software, you can stop a scan by performing either an orderly stop or an abrupt stop. In an orderly stop, the module finishes acquiring the data, stops all subsequent acquisition, and transfers the acquired data to host memory; all subsequent triggers or retriggers are ignored.

  In an abrupt stop, the module stops acquiring samples immediately; the acquired data is not transferred to host memory, and all subsequent triggers or retriggers are ignored.

Continuously Paced Scan Mode

Use continuously paced scan mode if you want to accurately control the period between conversions of individual channels in a scan.

When it detects an initial trigger, the module cycles through the channel-gain list, acquiring and converting the value for each entry in the list (this process is defined as the scan). The module then wraps to the start of the channel-gain list and repeats the process continuously until either the allocated buffers are filled or until you stop the operation. Refer to page 36 for more information on buffers.

The conversion rate is determined by the frequency of the A/D sample clock; refer to page 23 for more information on the A/D sample clock. The sample rate, which is the rate at which a single entry in the channel-gain list is sampled, is determined by the frequency of the A/D sample clock divided by the number of entries in the channel-gain list.

To select continuously paced scan mode, use software to specify the dataflow as continuous and to specify a trigger source to start the operation. Refer to page 25 for more information on the supported trigger sources.

Figure 3 illustrates continuously paced scan mode using a channel-gain list with three entries: channel 0, channel 1, and channel 2. In this example, analog input data is acquired on each clock pulse of the A/D sample clock. When it reaches the end of the channel-gain list, the module wraps to the beginning of the channel-gain list and repeats this process. Data is acquired continuously.

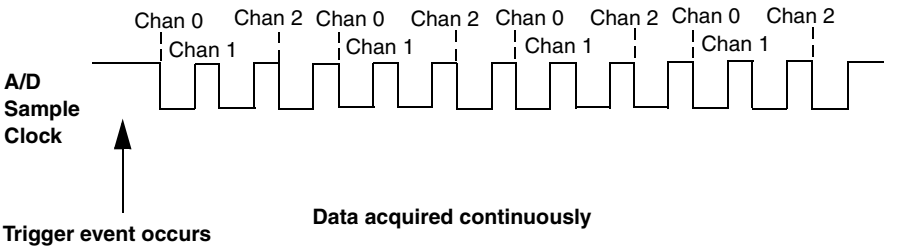


Figure 3: Continuously Paced Scan Mode

Triggered Scan Mode

DT9800 Series function modules support two triggered scan modes: internally retriggered and externally retriggered. These modes are described in the following subsections.

Internally Retriggered Scan Mode

Use internally retriggered scan mode if you want to accurately control both the period between conversions of individual channels in a scan and the period between each scan. This mode is useful when synchronizing or controlling external equipment or when acquiring a buffer of data on each trigger or retrigger.

When it detects an initial trigger (either a software trigger or an external trigger), the DT9800 Series function module scans the channel-gain list once, then waits for an internal retrigger to occur. When it detects an internal retrigger, the board scans the channel-gain list once again, then waits for another internal retrigger to occur. The process repeats continuously until either the allocated buffers are filled or until you stop the operation; refer to page 36 for more information on buffers.

The sample rate is determined by the frequency of the A/D sample clock divided by the number of entries in the channel-gain list; refer to page 23 for more information on the A/D sample clock. The conversion rate of each scan is determined by the frequency of the internal retrigger clock. The internal retrigger clock is the Triggered Scan Counter on the board; the Triggered Scan Counter is a 24-bit counter with a 12 MHz clock.

Figure 4 illustrates triggered scan mode. In this example, post-trigger analog input data is acquired on each clock pulse of the A/D sample clock until the channel-gain list has been scanned once; then, the board waits for the retrigger event. When the retrigger event occurs, the board scans the channel-gain list once again, acquiring data on each pulse of the A/D sample clock. The process repeats continuously with every specified retrigger event.

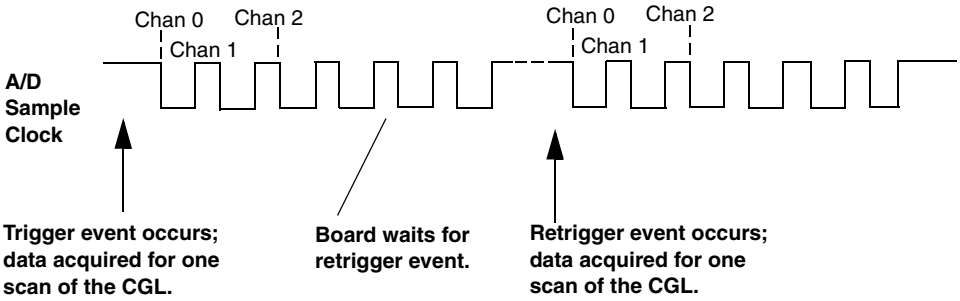


Figure 4: Triggered Scan Mode

Specify the frequency of the internal retrigger clock using software. The minimum retrigger frequency is 0.75 Hz (0.75 Samples/s); the maximum retrigger rate of each DT9800 Series function module is listed in Table 5 on page 30.

Table 5: Maximum Retrigger Frequency

Function Module Series	Module Name	Maximum Retrigger Frequency
DT9800 Standard	DT9801 DT9802 DT9803 DT9804	100 kHz
	DT9805[a] DT9806[a]	50 kHz
DT9800-MAC	DT9801-MAC DT9802-MAC DT9803-MAC DT9804-MAC	100 kHz
DT9800-EC	DT9801-EC DT9802-EC DT9803-EC DT9804-EC	100 kHz
DT9800-EC-I	DT9801-EC-I DT9802-EC-I DT9803-EC-I DT9804-EC-I	100 kHz

a. The maximum retrigger frequency is 50 kHz for a single channel or a channel scan when the gain is 1 or 10, 10 kHz for a channel scan when the gain is 100, and 2 kHz for a channel scan when the gain is 500.

The appropriate retrigger frequency depends on a number of factors, determined by the following equations:

$$\text{Min. Retrigger Period} = \frac{\text{\# of CGL entries}}{\text{A/D sample clock frequency}} + 2\ \mu s$$

$$\text{Max. Retrigger Frequency} = \frac{1}{\text{Min. Retrigger Period}}$$

For example, if you are using 16 channels in the channel-gain list, and using an A/D sample clock with a frequency of 50 kHz, set the maximum retrigger frequency to 3.106 kHz, since

$$3.106\ \text{kHz} = \frac{1}{\frac{16}{50\ \text{kHz}} + 2\ \mu\text{s}}$$

To select internally retriggered scan mode, use software to specify the following parameters:

- The dataflow as continuous;
- Triggered scan mode usage as enabled;
- The retrigger mode as internal;
- The number of times to scan per trigger or retrigger (also called the multiscan count) as 1;
- The frequency of the retrigger clock; and
- The initial trigger source; refer to page 25 for more information on the supported trigger sources.

Externally Retriggered Scan Mode

Use externally retriggered scan mode if you want to accurately control the period between conversions of individual channels and retrigger the scan based on an external event.

When a DT9800 Series function module detects an initial trigger (either a software trigger or an external trigger), the module scans the channel-gain list once, then waits for an external retrigger to occur. The external retrigger occurs when a rising edge is detected on the Ext A/D Trigger input screw terminal (TB24) on the module.

When the retrigger occurs, the module scans the channel-gain list once, then waits for another external retrigger to occur. The process repeats continuously until either the allocated buffers are filled (if buffer wrap mode is none) or until you stop the operation (if buffer wrap mode is single or multiple); refer to page 36 for more information on buffers.

The conversion rate of each channel is determined by the frequency of the A/D sample clock; refer to page 23 for more information on the A/D sample clock. The conversion rate of each scan is determined by the period between external retriggers; therefore, it cannot be accurately controlled. The module ignores external triggers that occur while it is acquiring data. Only external retrigger events that occur when the module is waiting for a retrigger are detected and acted on.

To select externally retriggered scan mode, use software to specify the following parameters:

- The dataflow as continuous;
- The triggered scan mode usage as enabled;
- The retrigger mode as an external retrigger (retrigger extra for DataAcq SDK users);
- The number of times to scan per trigger or retrigger (also called the multiscan count) to 1; and
- The retrigger source as the external trigger (external for DataAcq SDK users).

Note: For DataAcq SDK users, if you want to use the same trigger source as both the initial trigger and the retrigger source, specify the external trigger as the initial trigger source and specify the retrigger mode as scan-per-trigger. In this case, you need not specify the retrigger source; the module uses the initial trigger source as the retrigger source.

Data Format

Table 6 lists the data encoding used by each DT9800 Series function module.

Table 6: Data Encoding

Function Module Series	Module Name	Data Encoding
DT9800 Standard Series	DT9801 DT9802	Straight Binary
	DT9803 DT9804 DT9805 DT9806	Offset Binary
DT9800-MAC	DT9801-MAC DT9802-MAC	Straight Binary
	DT9803-MAC DT9804-MAC	Offset Binary
DT9800-EC	DT9801-EC DT9802-EC	Straight Binary
	DT9803-EC DT9804-EC	Offset Binary
DT9800-EC-I	DT9801-EC-I DT9802-EC-I	Straight Binary
	DT9803-EC-I DT9804-EC-I	Offset Binary

In software, the analog input value is returned as a code. To convert the code to voltage, use the following formulas:

$$LSB = \frac{FSR}{2^N}$$

$$Vin = Code * LSB + Offset$$

where,

- *LSB* is the least significant bit.
- *FSR* is the full-scale range. For the DT9800 Series, the full-scale range is 10 for the unipolar range or 20 for the bipolar range.
- *N* is the input resolution. Refer to Table 2 on page 13 for the list of input resolutions supported.
- *Vin* is the analog voltage.
- *Code* is the raw count used by the software to represent the voltage.
- *Offset* is the actual minus full-scale value. The minus full-scale value is 0.0 V for the unipolar input range and –10 V for the bipolar input range.

For example, assume that you are using a DT9801 with a unipolar input range. If the software returns a code of 2010 for the analog input operation, determine the analog input voltage as follows:

$$LSB = \frac{10}{4096} = 0.002441 \text{ V} + 0.0 \text{ V}$$

$$Vin = 2010 * 0.002441 + 0 \text{ V}$$

$$Vin = 4.906 \text{ V}$$

Similarly, assume that you are using a DT9804 board with a bipolar input range. The actual minus full-scale value is -10.0 V. If the software returns a code of 2010 for the analog input operation, determine the analog input voltage as follows:

$$LSB = \frac{20}{65536} = 0.000305 \text{ V}$$

Vin = 2010 * 0.000305 + -10.0 V

Vin = -9.370 V

Table 7 lists the values that are returned when the DT9800 Series function module is overrange.

Table 7: Overrange SIgnal Values

Function Module Series	Module Name	Above-Range Signals	Below-Range Signals
DT9800 Standard Series	DT9801 DT9802	FFFh (plus full-scale)	000h (minus full-scale)
	DT9803 DT9804 DT9805 DT9806	FFFFh (plus full-scale)	0000h (minus full-scale)
DT9800-MAC Series	DT9801-MAC DT9802-MAC	FFFh (plus full-scale)	000h (minus full-scale)
	DT9803-MAC DT9804-MAC	FFFFh (plus full-scale)	0000h (minus full-scale)
DT9800-EC Series	DT9801-EC DT9802-EC	FFFh (plus full-scale)	000h (minus full-scale)
	DT9803-EC DT9804-EC	FFFFh (plus full-scale)	0000h (minus full-scale)

Table 7: Overrange SIgnal Values (cont.)

Function Module Series	Module Name	Above-Range Signals	Below-Range Signals
DT9800-EC-I Series	DT9801-EC-I DT9802-EC-I	FFFh (plus full-scale)	000h (minus full-scale)
	DT9803-EC-I DT9804-EC-I	FFFFh (plus full-scale)	0000h (minus full-scale)

Data Transfer

The module packs two bytes into each transfer to the host computer. Even samples (corresponding to entries 0, 2, 4, and so on, in the channel-gain list) are packed into the low bytes; odd samples (corresponding to entries 1, 3, 5, and so on, in the channel-gain list) are packed into the high bytes.

DT9800 Series function modules contain a 2048-sample FIFO. During a continuous analog input operation, the hardware interrupts the firmware on the module when the FIFO is half full. The module then transfers 2048 samples to a circular buffer, which is dedicated to the hardware, in the host computer.

The DT9800 Series Device Driver accesses the hardware circular buffer to fill user buffers that you allocate in software. Keep the following recommendations in mind when allocating user buffers for continuous analog input operations on the DT9800 Series:

- Allocate a minimum of three user buffers.
- Specify a buffer size at least as large as the sampling rate; for example, if you are using a sampling rate of 100 kSamples/s (100 kHz), specify a buffer size of 100,000. The minimum buffer size that you should specify is 256 samples.

Note: If you are using a slow clock data rate, such as .75 Hz, and a 256 sample user buffer, you will have to wait over 5 minutes for any data since data is transferred only when 256 samples have been read.

- Specify one of the following buffer wrap modes:
  - If the wrap mode is none, data is written to the allocated buffers until no more empty buffers are available; at that point, the operation stops.
  - If wrap mode is multiple, data is written to the allocated multiple buffers continuously; when no more empty buffers are available, the module overwrites the data in the filled buffers starting with the first location of the first buffer. This process continues indefinitely until you stop it.
  - If wrap mode is single, data is written to a single buffer continuously; when the buffer is filled, the module overwrites the data in the buffer starting with the first location of the buffer. This process continues indefinitely until you stop it.

Error Conditions

The DT9800 Series function modules can report an error if one of the following conditions occurs:

- **A/D Over Sample error** –The A/D sample clock rate is too fast. This error is reported if a new A/D sample clock pulse occurs while the ADC is busy performing a conversion from the previous A/D sample clock pulse. The host computer can clear this error.

  To avoid this error, use a slower sampling rate.

- **A/D FIFO Full Flag set to 1** –The data was not read fast enough by the host computer. The host computer can clear this error. To avoid this error, ensure that you allocated at least three buffers, each at least as large as the sampling rate; for example, if you are using a sampling rate of 100 kSamples/s (100 kHz), specify a buffer size of 100,000 samples for each buffer.

  If one of these error conditions occurs, the module reports the error but continues to acquire and transfer data to the host computer.

Note: The LED on the front panel will not blink green if the hardware detects an error.

Analog Output Features

An analog output (D/A) subsystem is provided on the following DT9800 Series function modules only: DT9802, DT9802-MAC, DT9802-EC, DT9802-EC-I, DT9804, DT9804-MAC, DT9804-EC, DT9804-EC-I, and DT9806. This section describes the following features of the D/A subsystem:

- Output resolution, described on this page;
- Analog output channels, described on this page;
- Output ranges and gains, described on page 41;
- Conversion modes, described on page 42; and
- Data format, described on page 42.

Output Resolution

Table 2 lists the output resolution of the DT9800 Series function modules. Note that the resolution is fixed; it cannot be programmed in software.

Table 8: Output Resolution

Function Module Series	Module Name	Resolution
DT9800 Standard Series	DT9802	12 bit
	DT9804 DT9806	16 bit
DT9800-MAC Series	DT9802-MAC	12 bit
	DT9804-MAC	16 bit

Table 8: Output Resolution (cont.)

Function Module Series	Module Name	Resolution
DT9800-EC Series	DT9802-EC	12 bit
	DT9804-EC	16 bit
DT9800-EC-I Series	DT9802-EC-I	12 bit
	DT9804-EC-I	16 bit

Analog Output Channels

The DT9802, DT9802-MAC, DT9802-EC, DT9802-EC-I, DT9804, DT9804-MAC, DT9804-EC, DT9804-EC-I, and DT9806 modules support two DC-level analog output channels (DAC0 and DAC1). Refer to the *DT9800 Series Getting Started Manual* for information on how to wire analog output signals to the module using the screw terminal panel. You configure the channel type through software.

Within each DAC, the digital data is double-buffered to prevent spurious outputs, then output as an analog signal. Both DACs power up to a value of 0 V ±10 mV. Resetting the module does not clear the values in the DACs.

The DT9800 Series function modules can output data from a single analog output channel only. Specify the channel for a single-value analog output operation using software; refer to "Conversion Modes," on page 42 for more information on single-value operations.

Output Ranges and Gains

Table 9 lists the output range for each DT9800 Series function module.

Table 9: Output Range

Function Module Series	Module Name	Unipolar Output Range	Bipolar Input Range
DT9800 Standard Series	DT9802	0 to 10 V or 0 to 5 V	±10 V or ±5 V
	DT9804 DT9806	N/A	±10 V
DT9800-MAC Series	DT9802-MAC	0 to 10 V or 0 to 5 V	±10 V or ±5 V
	DT9804-MAC	N/A	±10 V
DT9800-EC Series	DT9802-EC	0 to 10 V or 0 to 5 V	±10 V or ±5 V
	DT9804-EC	N/A	±10 V
DT9800-EC-I Series	DT9802-EC-I	0 to 10 V or 0 to 5 V	±10 V or ±5 V
	DT9804-EC-I	N/A	±10 V

Specify the range using software; set the gain to 1.

Conversion Modes

DT9802, DT9802-MAC, DT9802-EC, DT9802-EC-I, DT9804, DT9804-MAC, DT9804-EC, DT9804-EC-I, and DT9806 modules can perform single-value analog output operations only. Use software to specify the range, gain, and analog output channel, then output the data from the specified channel. You cannot specify a clock source, trigger source, or buffer.

Note: You cannot perform a single-value analog output operation while the A/D subsystem is running.

The settling time for each DAC is 50 µs (20 V steps).

Single-value operations stop automatically when finished; you cannot stop a single-value operation.

Data Format

Data from the host computer must use offset binary data encoding for analog output signals. Using software, specify the data encoding as binary.

In software, you need to supply a code that corresponds to the analog output value you want the module to output. To convert a voltage to a code, use the following formulas:

$$LSB = \frac{FSR}{2^N}$$

$$Code = \frac{Vout - offset}{LSB}$$

where,

- *LSB* is the least significant bit.
- *FSR* is the full-scale range (10).
- *N* is the output resolution; see Table 8 on page 39 for a list of output resolutions.
- *Code* is the raw count used by the software to represent the voltage.
- *Vout* is the analog voltage.
- *Offset* is the minus full-scale value, or -10 V.

For example, assume that you are using a DT9804 module. If you want to output a voltage of 4.7 V, determine the code value as follows:

$$LSB = \frac{10\ V}{65536} = 0.0001526\ V$$

$$Code = \frac{4.7\ V - (-10\ V)}{0.0001526\ V}$$

Code = 96330 = 1784Ah

Digital I/O Features

This section describes the following features of the digital I/O subsystem:

- Digital I/O lines, described on this page;
- Resolution, described on this page; and
- Operation modes, described on page 45.

Digital I/O Lines

DT9800 Series function modules support eight digital input lines (Port A, lines 0 to 7) through the DIN subsystem and eight digital output lines (Port B, lines 0 to 7) through the DOUT subsystem.

For fast, clocked digital input operations, you can enter the digital input lines from Port A as channel 16 in the analog input channel list; refer to page 16 for more information.

The DT9800 Series function modules also provide a dynamic digital output line that you can update when an analog input channel is read. Note that the dynamic digital output line is in addition to the digital output lines in Port B. Refer to page 17 for more information on dynamic digital output operations.

On power up or module reset, no digital data is output from the modules. All the outputs include diode protection to the isolated ground and the isolated +5 V.

Note: DT9800-EC Series function modules do not provide isolated ground or isolated +5 V power.

Resolution

The resolution of the digital input port is fixed at 8 bits; the resolution of the digital output port is also fixed at 8 bits.

You cannot program the digital I/O resolution in software.

Operation Modes

The DT9800 Series function modules support the following digital I/O operation modes:

- **Single-value operations** are the simplest to use but offer the least flexibility and efficiency. You use software to specify the digital I/O port and a gain of 1 (the gain is ignored). Data is then read from or written to the digital I/O lines. For a single-value operation, you cannot specify a clock or trigger source.

  Single-value operations stop automatically when finished; you cannot stop a single-value operation.

- **Continuous digital input** takes full advantage of the capabilities of the DT9800 Series function modules. In this mode, enter all eight digital input lines of Port A as channel 16 of the analog input channel-gain list; program this mode through the A/D subsystem. Using this mode, you can specify a clock source, scan mode, trigger source, buffer, and buffer wrap mode for the digital input operation. Refer to page 16 for more information on specifying digital input lines for a continuous digital input operation.

- **Dynamic digital output** is useful for synchronizing and controlling external equipment and allows you to output data to the dynamic digital output line each time an analog input value is acquired. This mode is programmed through the A/D subsystem; refer to page 17 for more information.

Counter/Timer Features

The counter/timer circuitry on the module provides the clocking circuitry used by the A/D and D/A subsystems as well as several user counter/timer features. This section describes the following user counter/timer features:

- Units, described on this page;
- C/T clock sources, described on page 47;
- Gate types, described on page 49;
- Pulse types and duty cycles, described on page 51; and
- Counter/timer operation modes, described on page 53.

Units

Two 16-bit counter/timers are supported by all DT9800 Series modules. The counters are numbered 0 and 1.

Each counter accepts a clock input signal and gate input signal and outputs a clock output signal (also called a pulse output signal), as shown in Figure 5.

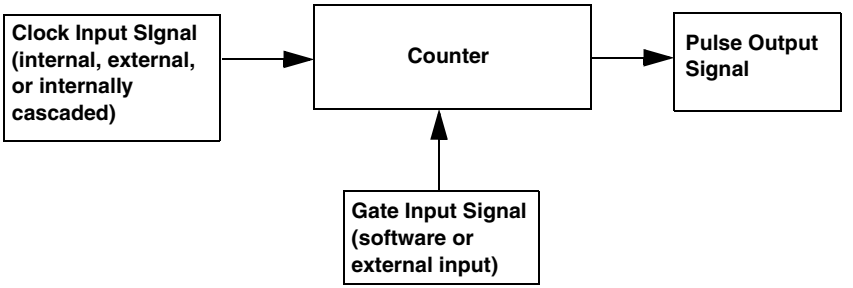

Clock Input SIgnal (internal, external, or internally cascaded)
Counter
Pulse Output Signal
Gate Input Signal (software or external input)

Figure 5: Counter/Timer Channel

Each counter corresponds to a counter/timer (C/T) subsystem. To specify the counter to use in software, specify the appropriate C/T subsystem. Counter 0 corresponds to C/T subsystem element 0; counter 1 corresponds to C/T subsystem element 1.

C/T Clock Sources

The following clock sources are available for the user counters:

- Internal C/T clock,
- External C/T clock, and
- Internally cascaded clock.

Refer to the following subsections for more information on these clock sources.

Internal C/T Clock

The internal C/T clock uses a 12 MHz time base. Counter/timer operations start on the rising edge of the clock input signal.

Through software, specify the clock source as internal and the frequency at which to pace the counter/timer operation (this is the frequency of the clock output signal). The maximum frequency that you can specify for the clock output signal is 750 kHz. The minimum frequency that you can specify for the clock output signal for each 16-bit counter is 183.1 Hz. The rising edge of the clock is the active edge.

External C/T Clock

An external C/T clock is useful when you want to pace counter/timer operations at rates not available with the internal C/T clock or if you want to pace at uneven intervals. The rising edge of the external C/T clock input signal is the active edge.

Using software, specify the clock source as external and the clock divider used to determine the frequency at which to pace the operation. The minimum clock divider that you can specify is 2.0; the maximum clock divider that you can specify is 65,536. For example, if you supply an external C/T clock with a frequency of 700 kHz and specify a clock divider of 2, the resulting frequency of the external C/T clock output signal is 350 kHz. The resulting frequency of the external C/T clock output signal must not exceed 750 kHz.

Table 10 on page 48 lists the screw terminals of the DT9800 Series modules that correspond to the external C/T clock signals of each counter/timer.

Table 10: External C/T Clock Signals

Module	Counter /Timer	Screw Terminal on Module	J1 Pin Number	Screw Terminal on AC1324 Panel	J5 Pin Number
DT9800 Standard Series; DT9800-MAC Series	0	TB54	54	–	–
	1	TB50	50	–	–
DT9800-EC Series; DT9800-EC-I Series	0	–	–	TB20	20
	1	–	–	TB16	16

Internally Cascaded Clock

You can also internally route the clock output signal from counter/timer 0 to the clock input signal of counter/timer 1 to internally cascade the counters. In this way, you can create a 32-bit counter without externally connecting two counters together.

Specify internal cascade mode in software. The rising edge of the clock input signal is active.

Through software, specify the clock source as internal and the frequency at which to pace the counter/timer operation (this is the frequency of the clock output signal). The maximum frequency that you can specify for the clock output signal is 750 kHz. For a 32-bit cascaded counter, the minimum frequency that you can specify for the clock output signal is 0.0028 Hz.

Gate Types

The active edge or level of the gate input to the counter enables counter/timer operations. The operation starts when the clock input signal is received. Specify the gate type in software.

DT9800 Series modules provide the following gate input types:

- **None** –A software command enables any specified counter/timer operation immediately after execution. This gate type is useful for all counter/timer modes; refer to page 53 for more information on these modes.
- **Logic-low level external gate input** –Enables a counter/timer operation when the external gate signal is low, and disables the counter/timer operation when the external gate signal is high. Note that this gate type is used only for event counting, frequency measurement, and rate generation; refer to page 53 for more information on these modes.
- **Logic-high level external gate input** –Enables a counter/timer operation when the external gate signal is high, and disables a counter/timer operation when the external gate signal is low. Note that this gate type is used only for event counting, frequency measurement, and rate generation; refer to page 53 for more information on these modes.

- **Falling-edge external gate input** –Enables a counter/timer operation on the transition from the high level to the low level (falling edge). In software, this is called a low-edge gate type. Note that this gate type is used only for one-shot and repetitive one-shot mode; refer to page 53 for more information on these modes.
- **Rising-edge external gate input** –Enables a counter/timer operation on the transition from the low level to the high level (rising edge). In software, this is called a high-edge gate type. Note that this gate type is used only for one-shot and repetitive one-shot mode; refer to page 61 for more information on these modes.

Table 11 lists the screw terminals and pin numbers on the DT9800 Series function modules that correspond to the gate input signals of each counter/timer.

Table 11: Gate Input Signals

Module	Counter /Timer	Screw Terminal on Module	J1 Pin Number	Screw Terminal on AC1324 Panel	J5 Pin Number
DT9800 Standard Series; DT9800-MAC Series	0	TB52	52	–	–
	1	TB48	48	–	–
DT9800-EC Series; DT9800-EC-I Series	0	–	–	TB18	18
	1	–	–	TB14	14

Pulse Output Types and Duty Cycles

DT9800 Series function modules can output pulses from each counter/timer. Table 12 lists the screw terminals of the modules that correspond to the pulse output signals of each counter/timer.

Table 12: Pulse Output Signals

Module	Counter /Timer	Screw Terminal on Module	J1 Pin Number	Screw Terminal on AC1324 Panel	J5 Pin Number
DT9800 Standard Series; DT9800-MAC Series	0	TB53	53	–	–
	1	TB49	49	–	–
DT9800-EC Series; DT9800-EC-I Series	0	–	–	TB19	19
	1	–	–	TB15	15

DT9800 Series function modules support the following pulse output types on the clock output signal:

- **High-to-low transitions** –The low portion of the total pulse output period is the active portion of the counter/timer clock output signal.
- **Low-to-high transitions** –The high portion of the total pulse output period is the active portion of the counter/timer pulse output signal.

You specify the pulse output type in software.

The duty cycle (or pulse width) indicates the percentage of the total pulse output period that is active. A duty cycle of 50, then, indicates that half of the total pulse is low and half of the total pulse output is high. You specify the duty cycle in software.

Note: The minimum pulse width must be 650 ns.

Figure 6 illustrates a low-to-high pulse with a duty cycle of approximately 30%.

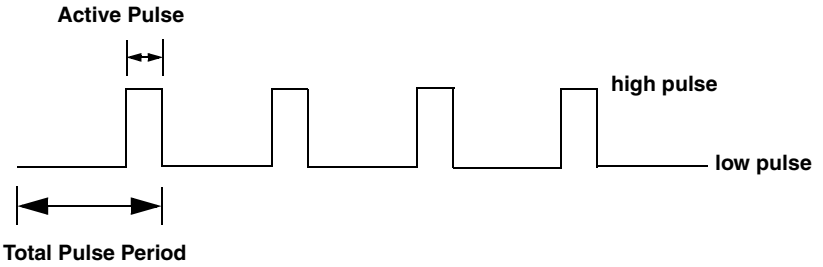


Figure 6: Example of a Low-to-High Pulse Output Type

Counter/Timer Operation Modes

DT9800 Series function modules support the following counter/timer operation modes:

- Event counting,
- Frequency measurement,
- Rate generation,
- One-shot, and
- Repetitive one-shot.

The following subsections describe these modes in more detail.

Event Counting

Use event counting mode to count events (clock pulses) from the counter's associated clock input source.

If you are using one counter, you can count a maximum of 65,536 events before the counter rolls over to 0 and starts counting again. If you are using a cascaded 32-bit counter, you can count a maximum of 4,294,967,296 events before the counter rolls over to 0 and starts counting again.

In event counting mode, use an external C/T clock source; refer to page 47 for more information on the external C/T clock source.

Using software, specify the counter/timer mode as event counting (count), the C/T clock source as external, and the gate type that enables the operation as logic high. Refer to page 51 for information on gates.

Ensure that the signals are wired appropriately. Refer to the *DT9800 Series Getting Started Manual* for wiring examples.

Figure 7 shows an example of an event counting operation using a logic-high gate type.

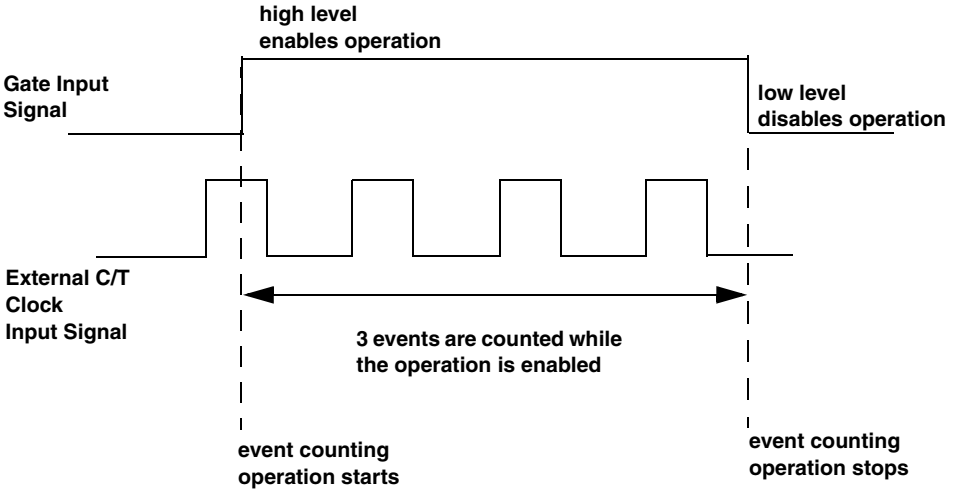


Figure 7: Example of Event Counting

Frequency Measurement

Use frequency measurement mode to measure the frequency of the signal from counter's associated clock input source over a specified duration. In this mode, use an external C/T clock source; refer to page 47 for more information on the external C/T clock source.

One way to perform a frequency measurement is to use the same wiring as an event counting application that does not use an external gate signal. Refer to the *DT9800 Series Getting Started Manual* for wiring examples.

In this configuration, use software to specify the counter/timer mode as frequency measurement or event counting (count), and the duration of the system timer over which to measure the frequency. (The system timer uses a resolution of 1 ms.) In this configuration, frequency is determined using the following equation:

$$\text{Frequency Measurement} = \frac{\text{Number of Events}}{\text{Duration of the System Timer}}$$

If you need more accuracy than the system timer provides, you can connect a pulse of a known duration (such as a one-shot output of another user counter) to the external gate input. Refer to the *DT9800 Series Getting Started Manual* for wiring examples.

In this configuration, use software to set up the counter/timers as follows:

1. Set up one of the counter/timers for one-shot mode, specifying the clock source, clock frequency, gate type, type of output pulse (high or low), and duty cycle.
2. Set up the counter/timer that will measure the frequency for event counting mode, specifying the clock source to count, and the gate type (this should match the pulse output type of the counter/timer set up for one-shot mode).
3. Start both counters (events are not counted until the active period of the one-shot pulse is generated).
4. Read the number of events counted. (Allow enough time to ensure that the active period of the one-shot occurred and that events have been counted.)
5. Determine the measurement period using the following equation:

$$\text{Measurement period} = \frac{1}{\text{Clock Frequency}} * \text{Active Pulse Width}$$

6. Determine the frequency of the clock input signal using the following equation:

$$\text{Frequency Measurement} = \frac{\text{Number of Events}}{\text{Measurement Period}}$$

Figure 8 shows an example of a frequency measurement operation. In this example, three events are counted during a duration of 300 ms. The frequency, then, is 10 Hz, since 10 Hz = 3/(.3 s).

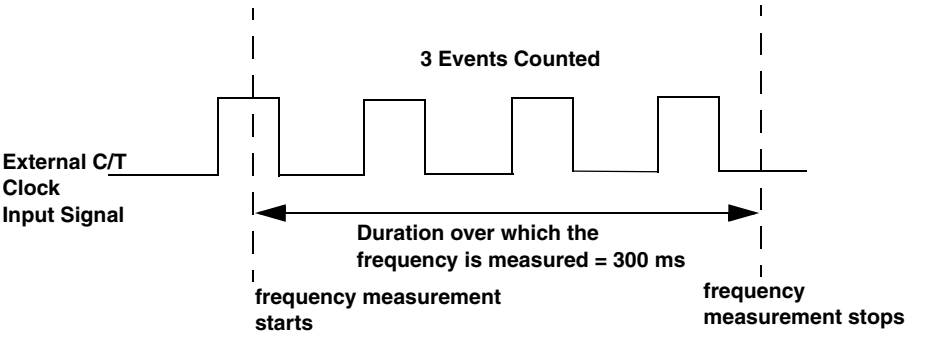


Figure 8: Example of Frequency Measurement

Rate Generation

Use rate generation mode to generate a continuous pulse output signal from the counter; this mode is sometimes referred to as continuous pulse output or pulse train output. You can use this pulse output signal as an external clock to pace other operations, such as analog input or other counter/timer operations.

While the pulse output operation is enabled, the counter outputs a pulse of the specified type and frequency continuously. As soon as the operation is disabled, rate generation stops.

The period of the output pulse is determined by the clock input signal and the external clock divider. If you are using one counter (not cascaded), you can output pulses using a maximum frequency of 1 MHz (this is the frequency of the clock output signal). In rate generation mode, either the internal or external C/T clock input source is appropriate depending on your application; refer to page 47 for more information on the C/T clock source.

Using software, specify the counter/timer mode as rate generation (rate), the C/T clock source as either internal or external, the polarity of the output pulses (high-to-low transitions or low-to-high transitions), the duty cycle of the output pulses, and the gate type that enables the operation as logic-high. Refer to page 51 for more information on pulse output signals and to page 49 for more information on gate types.

Ensure that the signals are wired appropriately. Refer to the *DT9800 Series Getting Started Manual* for wiring examples.

Figure 9 shows an example of an enabled rate generation operation using a logic-high gate input signal, an external C/T clock source with an input frequency of 4 kHz, a clock divider of 4, a low-to-high pulse type, and a duty cycle of 75%. A 1 kHz square wave is the generated output. Figure 10 shows the same example using a duty cycle of 25%.

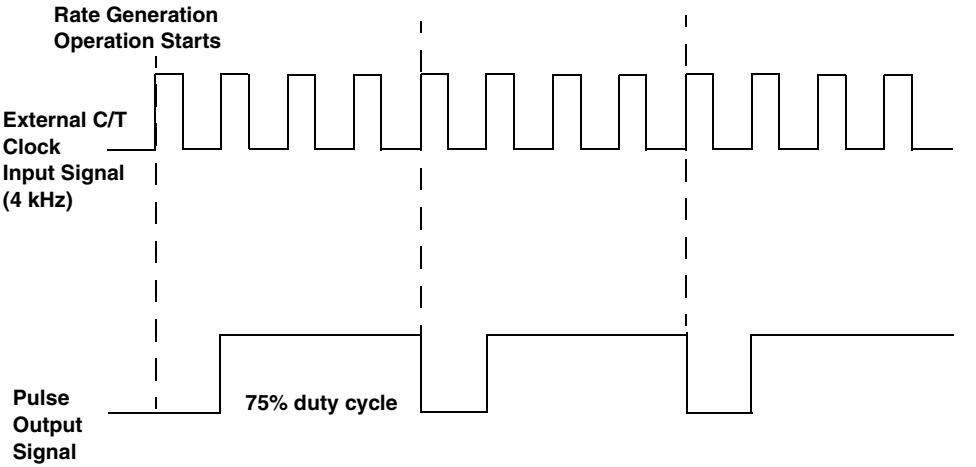


Figure 9: Example of Rate Generation Mode with a 75% Duty Cycle

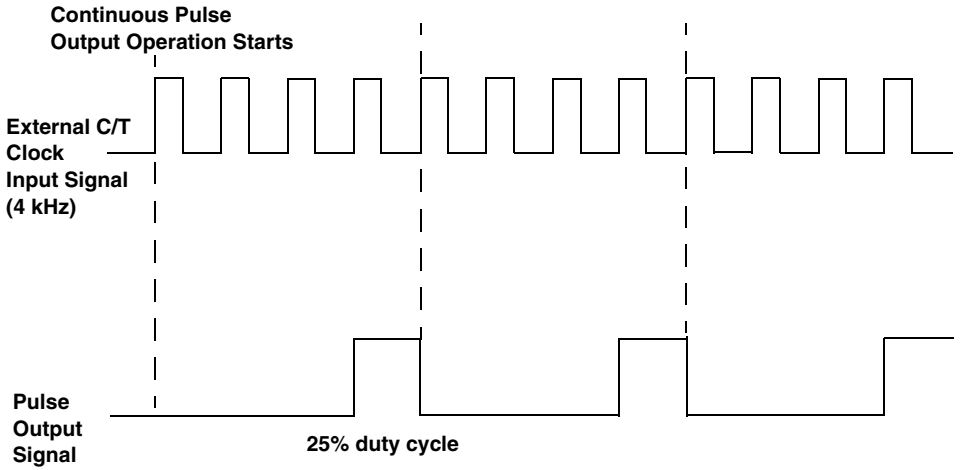


Figure 10: Example of Rate Generation Mode with a 25% Duty Cycle

One-Shot

Use one-shot mode to generate a single pulse output signal from the counter when the operation is triggered (determined by the gate input signal). You can use this pulse output signal as an external digital (TTL) trigger to start other operations, such as analog input operations.

When the one-shot operation is triggered, a single pulse is output; then, the one-shot operation stops. All subsequent clock input signals and gate input signals are ignored.

The period of the output pulse is determined by the clock input signal. In one-shot mode, the internal C/T clock source is more useful than an external C/T clock source; refer to page 47 for more information on the internal C/T clock source.

Using software, specify the counter/timer mode as one-shot, the clock source as internal, the polarity of the output pulse (high-to-low transition or low-to-high transition), the duty cycle of the output pulse, and the gate type to trigger the operation as rising edge or falling edge. Refer to page 51 for more information on pulse output types and to page 49 for more information on gate types.

Note: In the case of a one-shot operation, use a duty cycle as close to 100% as possible to output a pulse immediately. Using a duty cycle closer to 0% acts as a pulse output delay.

Ensure that the signals are wired appropriately. Refer to the *DT9800 Series Getting Started Manual* for wiring examples.

Figure 11 shows an example of a one-shot operation using an external gate input (rising edge), a clock output frequency of 1 kHz (pulse period of 1 ms), a low-to-high pulse type, and a duty cycle of 99.99%. Figure 12 shows the same example using a duty cycle of 50%.

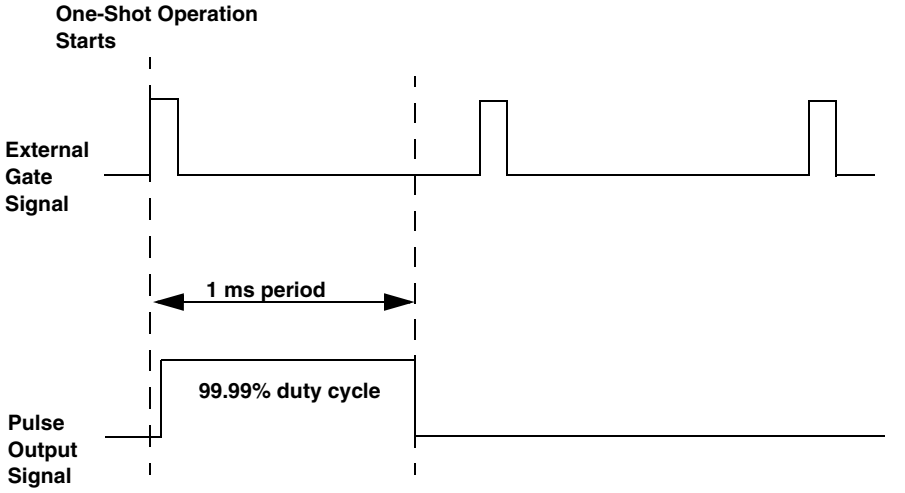


Figure 11: Example of One-Shot Mode Using a 99.99% Duty Cycle

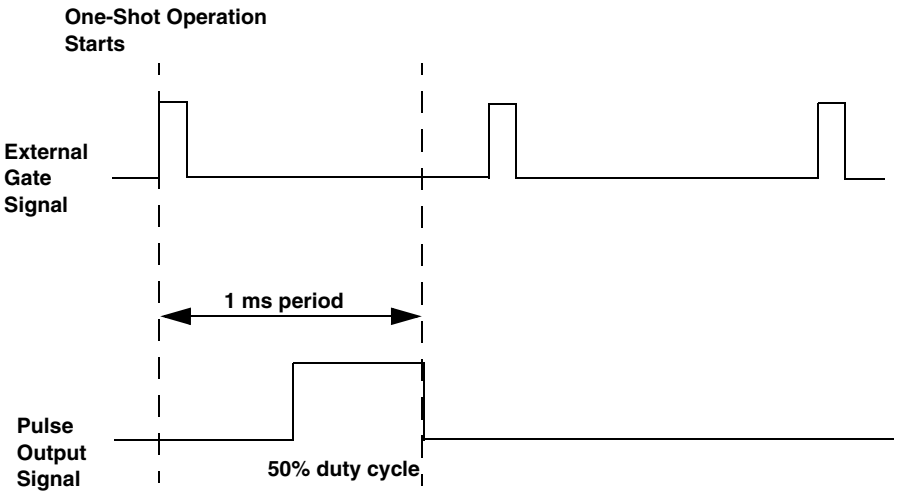


Figure 12: Example of One-Shot Mode Using a 50% Duty Cycle

Repetitive One-Shot

Use repetitive one-shot mode to generate a pulse output signal each time the module detects a trigger (determined by the gate input signal). You can use this mode to clean up a poor clock input signal by changing its pulse width, then outputting it.

In repetitive one-shot mode, the internal C/T clock source is more useful than an external C/T clock source; refer to page 47 for more information on the internal C/T clock source.

Use software to specify the counter/timer mode as repetitive one-shot (oneshot-rpt for SDK users), the polarity of the output pulses (high-to-low transitions or low-to-high transitions), the duty cycle of the output pulses, the C/T clock source, and the gate type to trigger the operation as rising edge or falling edge. Refer to page 51 for more information on pulse output types and to page 49 for more information on gates.

Note: In the case of a one-shot operation, use a duty cycle as close to 100% as possible to output a pulse immediately. Using a duty cycle closer to 0% acts as a pulse output delay.

When the one-shot operation is triggered (determined by the gate input signal), a pulse is output. When the module detects the next trigger, another pulse is output. This operation continues until you stop the operation.

Note: Triggers that occur while the pulse is being output are not detected by the module.

Ensure that the signals are wired appropriately. Refer to the *DT9800 Series Getting Started Manual* for wiring examples.

Figure 13 shows an example of a repetitive one-shot operation using an external gate (rising edge); a clock output frequency of 1 kHz (one pulse every 1 ms), a low-to-high pulse type, and a duty cycle of 99.99%. Figure 14 shows the same example using a duty cycle of 50%.

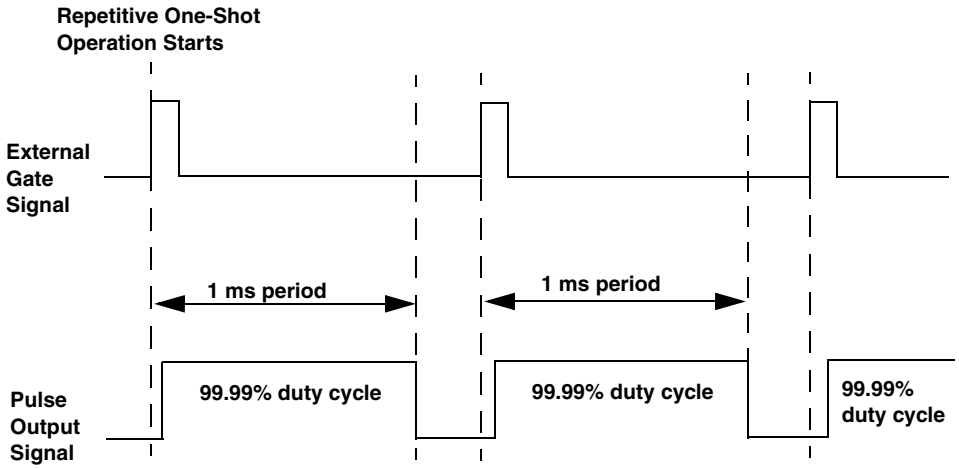


Figure 13: Example of Repetitive One-Shot Mode Using a 99.99% Duty Cycle

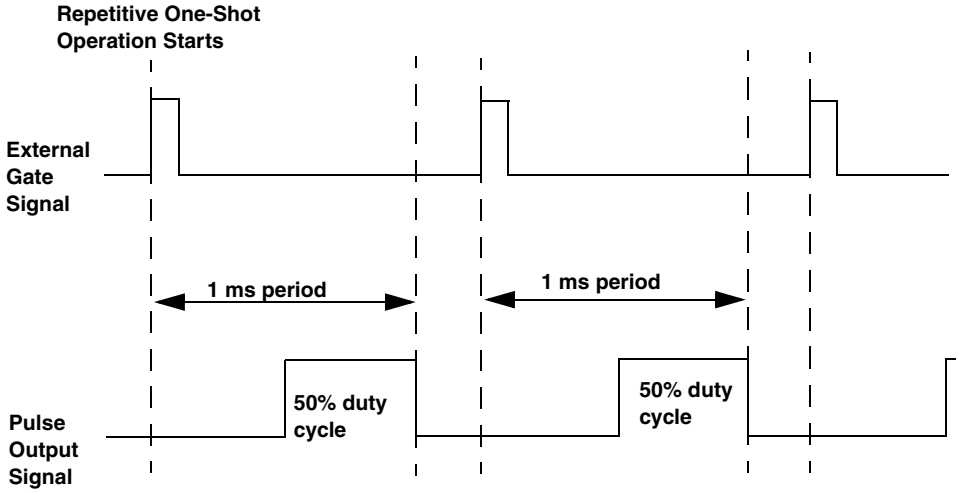


Figure 14: Example of Repetitive One-Shot Mode Using a 50% Duty Cycle

Supported Device Driver Capabilities

The DT9800 Series Device Driver provides support for A/D, D/A, DIN, DOUT, and C/T subsystems. For information on how to configure the device driver, refer to the *DT9800 Series Getting Started Manual.*

Table 13 summarizes the features available for use with the DataAcq SDK and the DT9800 Series function modules. The DataAcq SDK provides functions that return support information for specified subsystem capabilities at run-time.

The first row in the table lists the subsystem types. The first column in the table lists all possible subsystem capabilities. A description of each capability is followed by the parameter used to describe that capability in the DataAcq SDK.

Note: Blank fields represent unsupported options.

The DataAcq SDK uses the functions **olDaGetSSCaps** (for those queries starting with OLSSC) and **olDaGetSSCapsEx** (for those queries starting with OLSSCE) to return the supported subsystem capabilities for a device.

For more information, refer to the description of these functions in the DataAcq SDK online help. See the *DataAcq User's Manual* for information on launching this help file.

Table 13: DT9800 Series Supported Options

	DT9800 Series	A/D	D/A[a]	DIN	DOUT	SRL	C/T
	Total Subsystems on Module	**1**	**1**	**1**	**1**	**0**	**2**
Data Flow Mode	Single-Value Operation Support OLSSC_SUP_SINGLEVALUE	Yes	Yes	Yes[b]	Yes		
	Continuous Operation Support OLSSC_SUP_CONTINUOUS	Yes					Yes
	Continuous Operation until Trigger Event Support OLSSC_SUP_CONTINUOUS_PRETRIG						
	Continuous Operation before and after Trigger Event OLSSC_SUP_CONTINUOUS_ABOUTTRIG						
	DT-Connect Support OLSSC_SUP_DTCONNECT						
	Continuous DT-Connect Support OLSSC_SUP_DTCONNECT_CONTINUOUS						
	Burst DT-Connect Support OLSSC_SUP_DTCONNECT_BURST						
Sim. Oper.	Simultaneous Start List Support OLSSC_SUP_SIMULTANEOUS_START						
Pause Oper.	Pause Operation Support OLSSC_SUP_PAUSE						
Wind. Mess.	Asynchronous Operation Support OLSSC_SUP_POSTMESSAGE	Yes					

Table 13: DT9800 Series Supported Options (cont.)

	DT9800 Series	A/D	D/A[a]	DIN	DOUT	SRL	C/T
	Total Subsystems on Module	**1**	**1**	**1**	**1**	**0**	**2**
Buffering	Buffer Support OLSSC_SUP_BUFFERING	Yes					
	Single Buffer Wrap Mode Support OLSSC_SUP_WRPSINGLE	Yes					
	Multiple Buffer Wrap Mode Support OLSSC_SUP_WRPMULTIPLE	Yes					
	Inprocess Buffer Flush Support OLSSC_SUP_INPROCESSFLUSH	Yes					
DMA	Number of DMA Channels OLSSC_NUMDMACHANS	0	0	0	0		0
	Supports Gap Free Data with No DMA OLSSC_SUP_GAPFREE_NODMA	Yes					
	Supports Gap Free Data with Single DMA OLSSC_SUP_GAPFREE_SINGLEDMA						
	Supports Gap Free Data with Dual DMA OLSSC_SUP_GAPFREE_DUALDMA						
Triggered Scan Mode	Triggered Scan Support OLSSC_SUP_TRIGSCAN	Yes					
	Maximum Number of CGL Scans per Trigger OLSSC_MAXMULTISCAN	1	0	0	0		0
	Supports Scan per Trigger Event Triggered Scan OLSSC_SUP_RETRIGGER_SCAN_PER_TRIGGER	Yes					
	Supports Internal Retriggered Triggered Scan OLSSC_SUP_RETRIGGER_INTERNAL	Yes					
	Extra Retrigger Support OLSSC_SUP_RETRIGGER_EXTRA	Yes					

Table 13: DT9800 Series Supported Options (cont.)

	DT9800 Series	A/D	D/A[a]	DIN	DOUT	SRL	C/T
	Total Subsystems on Module	**1**	**1**	**1**	**1**	**0**	**2**
Triggered Scan Mode (cont.)	Maximum Retrigger Frequency OLSSCE_MAXRETRIGGER	100 kHz, 50 kHz[c]	0	0	0		0
	Minimum Retrigger Frequency OLSSCE_MINRETRIGGER	0.75 Hz[d]	0	0	0		0
Channel-Gain List	Maximum Channel Gain List Depth OLSSC_CGLDEPTH	32	0	0	0		0
	Sequential Channel Gain List Support OLSSC_SUP_SEQUENTIAL_CGL	Yes					
	Zero Start Sequential Channel Gain List Support OLSSC_SUP_ZEROSEQUENTIAL_CGL	Yes					
	Random Channel-Gain List Support OLSSC_SUP_RANDOM_CGL	Yes					
	Simultaneous Sample and Hold Support OLSSC_SUP_SIMULTANEOUS_SH						
	Channel List Inhibit Support OLSSC_SUP_CHANNELLIST_INHIBIT						
Gain	Programmable Gain Support OLSSC_SUP_PROGRAMGAIN	Yes					
	Number of Gains OLSSC_NUMGAINS	4[e]	1	1	1		0
	Autoranging OLSSC_SINGLEVALUE_AUTORANGE	Yes[f]					

Table 13: DT9800 Series Supported Options (cont.)

	DT9800 Series	A/D	D/A[a]	DIN	DOUT	SRL	C/T
	Total Subsystems on Module	**1**	**1**	**1**	**1**	**0**	**2**
Synchronous Digital I/O	Synchronous Digital I/O Support OLSSC_SUP_SYNCHRONOUS_DIGITALIO	Yes					
	Maximum Synchronous Digital I/O Value OLSSC_MAX_DIGITALIOLIST_VALUE	1	0	0	0		0
I/O Channels	Number of Channels OLSSC_NUMCHANNELS	9 or 17[g]	2	1	1		1
	DT2896 Channel Expansion Support OLSSC_SUP_EXP2896						
	DT727 Channel Expansion OLSSC_SUP_EXP727						
Channel Type	SE Support OLSSC_SUP_SINGLEENDED	Yes					
	SE Channels OLSSC_MAXSECHANS	16	0	0	0		0
	DI Support OLSSC_SUP_DIFFERENTIAL	Yes	Yes	Yes	Yes		Yes
	DI Channels OLSSC_MAXDICHANS	8	2	1	1		1
Filters	Filter/Channel Support OLSSC_SUP_FILTERPERCHAN						
	Number of Filters OLSSC_NUMFILTERS	1	1	1	1		0
Ranges	Number of Voltage Ranges OLSSC_NUMRANGES	2[h]	4[i]	0	0		0
	Range per Channel Support OLSSC_SUP_RANGEPERCHANNEL						

Table 13: DT9800 Series Supported Options (cont.)

	DT9800 Series	A/D	D/A[a]	DIN	DOUT	SRL	C/T
	Total Subsystems on Module	**1**	**1**	**1**	**1**	**0**	**2**
Resolution	Software Programmable Resolution OLSSC_SUP_SWRESOLUTION						
	Number of Resolutions OLSSC_NUMRESOLUTIONS	1	1	1	1		1
Data Encoding	Binary Encoding Support OLSSC_SUP_BINARY	Yes	Yes	Yes	Yes		Yes
	Twos Complement Support OLSSC_SUP_2SCOMP						
Triggers	Software Trigger Support OLSSC_SUP_SOFTTRIG	Yes	Yes	Yes	Yes		Yes
	External Trigger Support OLSSC_SUP_EXTERNTRIG	Yes[j]					Yes
	Positive Threshold Trigger Support OLSSC_SUP_THRESHTRIGPOS						
	Negative Threshold Trigger Support OLSSC_SUP_THRESHTRIGNEG						
	Analog Event Trigger Support OLSSC_SUP_ANALOGEVENTTRIG						
	Digital Event Trigger Support OLSSC_SUP_DIGITALEVENTTRIG						
	Timer Event Trigger Support OLSSC_SUP_TIMEREVENTTRIG						
	Number of Extra Triggers OLSSC_NUMEXTRATRIGGERS	0	0	0	0		0

Table 13: DT9800 Series Supported Options (cont.)

	DT9800 Series	A/D	D/A[a]	DIN	DOUT	SRL	C/T
	Total Subsystems on Module	**1**	**1**	**1**	**1**	**0**	**2**
Clocks	Internal Clock Support OLSSC_SUP_INTCLOCK	Yes	Yes				Yes
	External Clock Support OLSSC_SUP_EXTCLOCK	Yes					Yes
	Number of Extra Clocks OLSSC_NUMEXTRACLOCKS	0	0	0	0		0
	Base Clock Frequency OLSSCE_BASECLOCK	12 MHz	0	0	0		12 MHz
	Maximum External Clock Divider OLSSCE_MAXCLOCKDIVIDER	1.0	1.0	1.0	1.0		65536
	Minimum External Clock Divider OLSSCE_MINCLOCKDIVIDER	1.0	1.0	1.0	1.0		2.0
	Maximum Throughput OLSSCE_MAX_THROUGHPUT	100 kHz[k]	0		0		750 kHz
	Minimum Throughput OLSSCE_MIN_THROUGHPUT	0.75 Hz	1.0	0	0		.0028 Hz[l]
Counter/Timers	Cascading Support OLSSC_SUP_CASCADING						Yes
	Event Count Mode Support OLSC_SUP_CTMODE_COUNT						Yes
	Generate Rate Mode Support OLSSC_SUP_CTMODE_RATE						Yes
	One-Shot Mode Support OLSSC_SUP_CTMODE_ONESHOT						Yes
	Repetitive One-Shot Mode Support OLSSC_SUP_CTMODE_ONESHOT_RPT						Yes
	High to Low Output Pulse Support OLSSC_SUP_PLS_HIGH2LOW						Yes

Table 13: DT9800 Series Supported Options (cont.)

	DT9800 Series	A/D	D/A[a]	DIN	DOUT	SRL	C/T
	Total Subsystems on Module	**1**	**1**	**1**	**1**	**0**	**2**
Counter/Timers	Low to High Output Pulse Support OLSSC_SUP_PLS_LOW2HIGH						Yes
	None (internal) Gate Type Support OLSSC_SUP_GATE_NONE						Yes
	High Level Gate Type Support OLSSC_SUP_GATE_HIGH_LEVEL						Yes[m]
	Low Level Gate Type Support OLSSC_SUP_GATE_LOW_LEVEL						Yes[m]
	High Edge Gate Type Support OLSSC_SUP_GATE_HIGH_EDGE						Yes[m]
	Low Edge Gate Type Support OLSSC_SUP_GATE_LOW_EDGE						Yes[m]
	Level Change Gate Type Support OLSSC_SUP_GATE_LEVEL						
	High Level Gate Type with Input Debounce Support OLSSC_SUP_GATE_HIGH_LEVEL_DEBOUNCE						
	Low Level Gate Type with Input Debounce Support OLSSC_SUP_GATE_LOW_LEVEL_DEBOUNCE						
	High Edge Gate Type with Input Debounce Support OLSSC_SUP_GATE_HIGH_EDGE_DEBOUNCE						

Table 13: DT9800 Series Supported Options (cont.)

	DT9800 Series	A/D	D/A[a]	DIN	DOUT	SRL	C/T
	Total Subsystems on Module	**1**	**1**	**1**	**1**	**0**	**2**
Counter/Timers (cont.)	Low Edge Gate Type with Input Debounce Support OLSSC_SUP_GATE_LOW_EDGE_DEBOUNCE Level Change Gate Type with Input Debounce Support OLSSC_SUP_GATE_LEVEL_DEBOUNCE						
Interrupt	Interrupt Support OLSSC_SUP_INTERRUPT						
FIFOs	FIFO in Data Path Support OLSSC_SUP_FIFO						
Processor	Data Processing Capability OLSSC_SUP_PROCESSOR						
Software Calibration	Software Calibration Support OLSSC_SUP_SWCAL	Yes	Yes				

a. D/A subsystems are supported by the DT9802, DT9802-MAC, DT9802-EC, DT9802-EC-I, DT9804, DT9804-MAC, DT9804-EC, DT9804-EC-I, and DT9806 modules only.

b. While the DIN subsystem itself is incapable of continuous operation, you can perform a continuous DIN operation by specifying channel 16 in the channel-gain list of the A/D subsystem and starting the A/D subsystem. All 8 bits of the digital input lines from Port A are assigned to A/D input channel 16.

c. The maximum retrigger frequency for all modules except the DT9805 and DT9806 is 100 kHz. The DT9805 and DT9806 modules support a maximum retrigger frequency of 50 kHz. The appropriate retrigger frequency to use depends on the number of samples in the channel-gain list and the A/D sample clock frequency, as follows:

$$\text{Min. Retrigger Period} = \frac{\text{\# of CGL entries}}{\text{A/D sample clock frequency}} + 2\ \mu s$$

$$\text{Max. Retrigger Frequency} = \frac{1}{\text{Min. Retrigger Period}}$$

d. The value of 0.75 Hz assumes the minimum number of samples is 1.

e. The DT9805 and DT9806 function modules support gains of 1, 10, 100, and 500; all other DT9800 Series function modules support gains of 1, 2, 4, and 8.
f. Autoranging is supported in single-value mode only for the DT9805 and DT9806. Refer to page 26 for more information on autoranging.
g. Channels 0 to 15 are provided for single-ended analog inputs; channels 0 to 7 are provided for differential inputs. Channel 16 reads all 8 bits from the DIN subsystem (Port A).
h. DT9801, DT9801-MAC, DT9801-EC, DT9801-EC-I, DT9802, DT9802-MAC, DT9802-EC, and DT9802-EC-I modules support input ranges of 0 to 10 V or ±10 V. DT9803, DT9803-MAC, DT9803-EC, DT9803-EC-I, DT9804, DT9804-MAC, DT9804-EC, DT9804-EC-I, DT9805, and DT9806 modules support an input range of ±10 V only.
i. DT9802, DT9802-MAC, DT9802-EC, and DT9802-EC-I modules support an output range of 0 to 10 V, 0 to 5 V, ±10 V, or 0 to 10 V. DT9804, DT9804-MAC, DT9804-EC, DT9804-EC-I, and DT9806 modules support an output range of ±10 V only.
j. The external trigger is the rising-edge External A/D Trigger input.
k. The maximum throughput for analog input channels is 100 kHz for all modules except the DT9805 and DT9806 modules. The maximum throughput for the DT9805 and DT9806 modules is 50 kHz for a single channel or channel scan with gains of 1 and 10, 10 kHz for a channel scan with a gain of 100, and 2 kHz for a channel scan and a gain of 500.
l. Counter/timers 0 and 1 can be cascaded. If you are not using cascaded timers, this value is approximately 183 Hz.
m. High-edge and low-edge are supported for one-shot and repetitive one-shot modes. High-level and low-level are supported for event counting and rate generation modes.

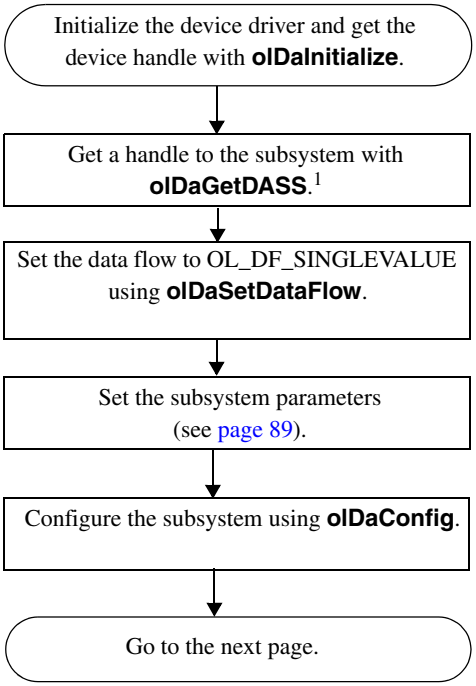
Programming Flowcharts

Single-Value Operations 79
Continuous A/D Operations 81
Event Counting Operations 83
Frequency Measurement Operations 85
Pulse Output Operations. 87

The following flowcharts show the steps required to perform data acquisition operations using DT-Open Layers. For illustration purposes, the DataAcq SDK functions are shown; however, the concepts apply to all DT-Open Layers software.

Note that many steps represent several substeps; if you are unfamiliar with the detailed operations involved with any one step, refer to the indicated page for detailed information. Optional steps appear in shaded boxes.

Single-Value Operations


Initialize the device driver and get the device handle with **olDaInitialize**.
Get a handle to the subsystem with **olDaGetDASS**.[1]
Set the data flow to OL_DF_SINGLEVALUE using **olDaSetDataFlow**.
Set the subsystem parameters (see page 89).
Configure the subsystem using **olDaConfig**.
Go to the next page.

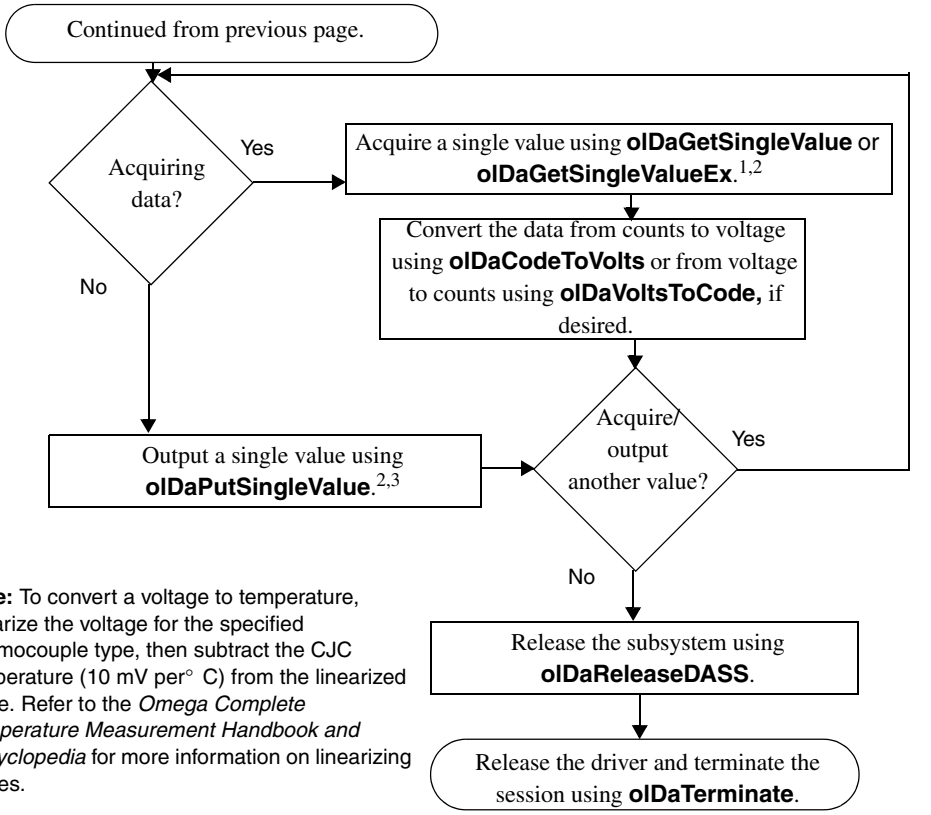
Specify A/D for an analog input subsystem or for digital channel 16 (which corresponds to the digital input port), D/A for an analog output subsystem, DIN for a digital input subsystem, or DOUT for a digital output subsystem.

Note that you cannot perform a single-value analog output operation while the A/D subsystem is running.

4

[1] For the DIN subsystem, element 0 corresponds to Port A (lines 0 to 7), for the DOUT subsystem, element 0 corresponds to Port B (lines 0 to 7).

Single-Value Operations (cont.)


Continued from previous page.
Acquiring data?
Yes
No
Acquire a single value using **olDaGetSingleValue** or **olDaGetSingleValueEx**.[1,2]
Convert the data from counts to voltage using **olDaCodeToVolts** or from voltage to counts using **olDaVoltsToCode,** if desired.
Acquire/ output another value?
Yes
No
Output a single value using **olDaPutSingleValue**.[2,3]
Release the subsystem using **olDaReleaseDASS**.
Release the driver and terminate the session using **olDaTerminate**.

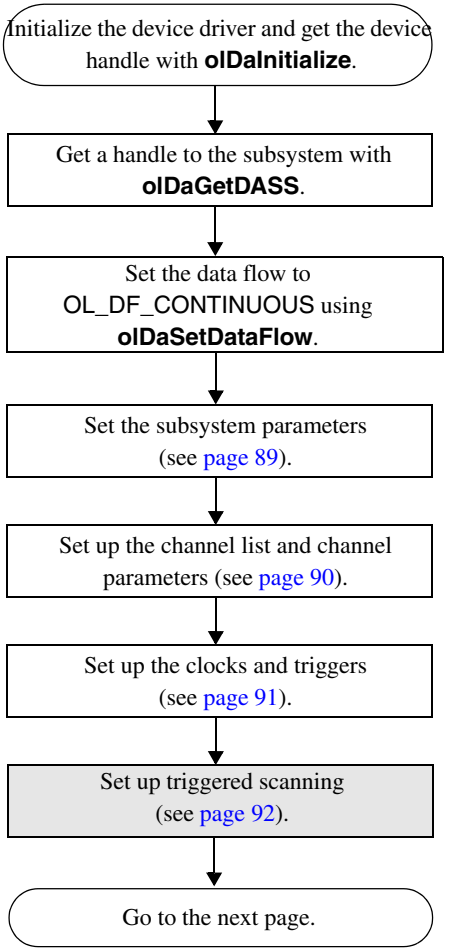
Note: To convert a voltage to temperature, linearize the voltage for the specified thermocouple type, then subtract the CJC temperature (10 mV per° C) from the linearized value. Refer to the *Omega Complete Temperature Measurement Handbook and Encyclopedia* for more information on linearizing values.

[1] Analog input channels range from 0 to 15 for single-ended and pseudo-differential configurations or 0 to 7 for the differential configuration using the specified gain (1, 2, 4, or 8 for all modules except the DT9805 and DT9806, which support gains of 1, 10, 100, and 500). If you use **olDaGetSingleValueEx**, the board can determine the best gain to use for the range (autorange is True); the value is returned in both counts and voltage.

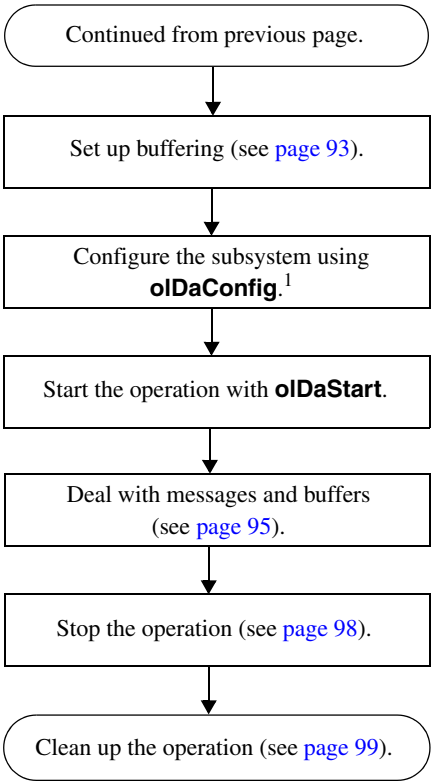
[2] Eight digital input lines (0 to 7) are available on Port A, and eight digital output lines (0 to 7) are available on Port B.

[3] The value is output to the specified analog output channel (DAC 0 or 1) or to a digital output line using a gain of 1.

Continuous A/D Operations


Initialize the device driver and get the device handle with **olDaInitialize**.
Get a handle to the subsystem with **olDaGetDASS**.
Set the data flow to OL_DF_CONTINUOUS using **olDaSetDataFlow**.
Set the subsystem parameters (see page 89).
Set up the channel list and channel parameters (see page 90).
Set up the clocks and triggers (see page 91).
Set up triggered scanning (see page 92).
Go to the next page.

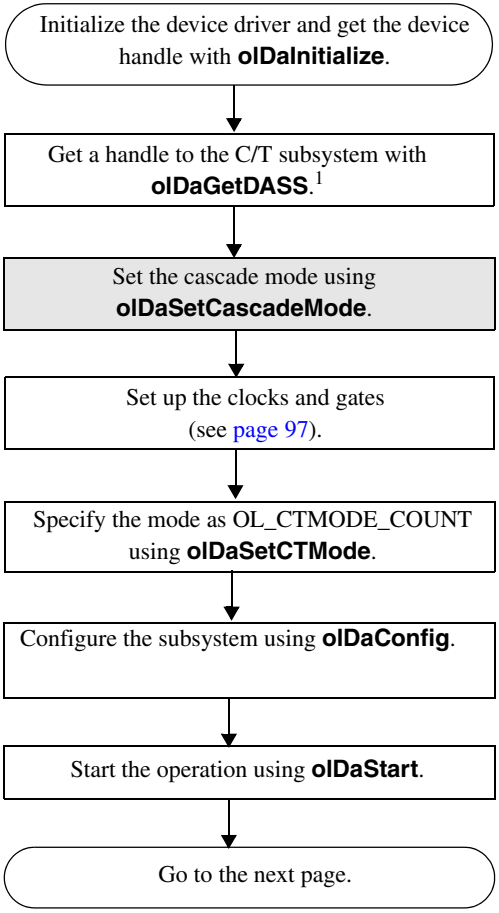
Continuous A/D Operations (cont.)


Continued from previous page.
Set up buffering (see page 93).
Configure the subsystem using **olDaConfig**.[1]
Start the operation with **olDaStart**.
Deal with messages and buffers (see page 95).
Stop the operation (see page 98).
Clean up the operation (see page 99).

Note: To convert a voltage to temperature, linearize the voltage for the specified thermocouple type, then subtract the CJC temperature (10 mV per° C) from the linearized value. Refer to the *Omega Complete Temperature Measurement Handbook and Encyclopedia* for more information on linearizing values.

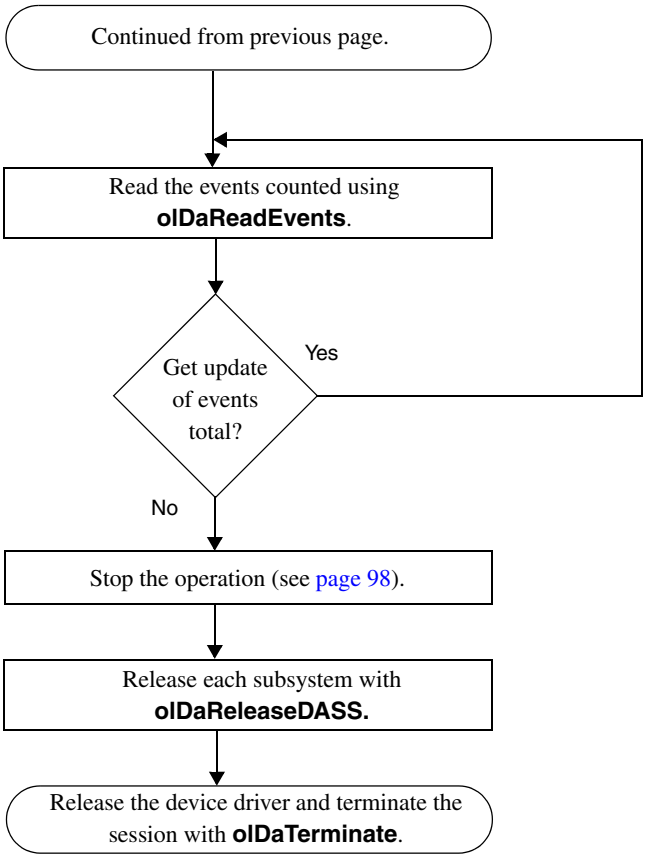
[1] After configuration, if using an internal clock, you can use **olDaGetClockFrequency** to get the actual frequency that the internal pacer clock could achieve; if using internal retrigger mode, you can use **olDaGetRetriggerFrequency** to get the actual frequency that the internal retrigger clock could achieve.

Event Counting Operations


Initialize the device driver and get the device handle with **olDaInitialize**.
Get a handle to the C/T subsystem with **olDaGetDASS**.[1]
Set the cascade mode using **olDaSetCascadeMode**.
Set up the clocks and gates (see page 97).
Specify the mode as OL_CTMODE_COUNT using **olDaSetCTMode**.
Configure the subsystem using **olDaConfig**.
Start the operation using **olDaStart**.
Go to the next page.

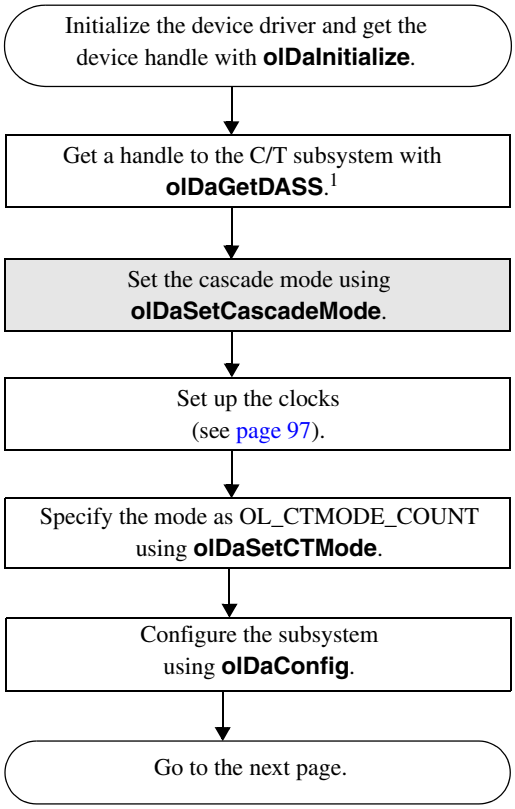
[1] Specify the appropriate C/T subsystem/element. The Windows device driver supports two elements (0 and 1).

Event Counting Operations (cont.)


Continued from previous page.
Read the events counted using **olDaReadEvents**.
Get update of events total?
Yes
No
Stop the operation (see page 98).
Release each subsystem with **olDaReleaseDASS.**
Release the device driver and terminate the session with **olDaTerminate**.

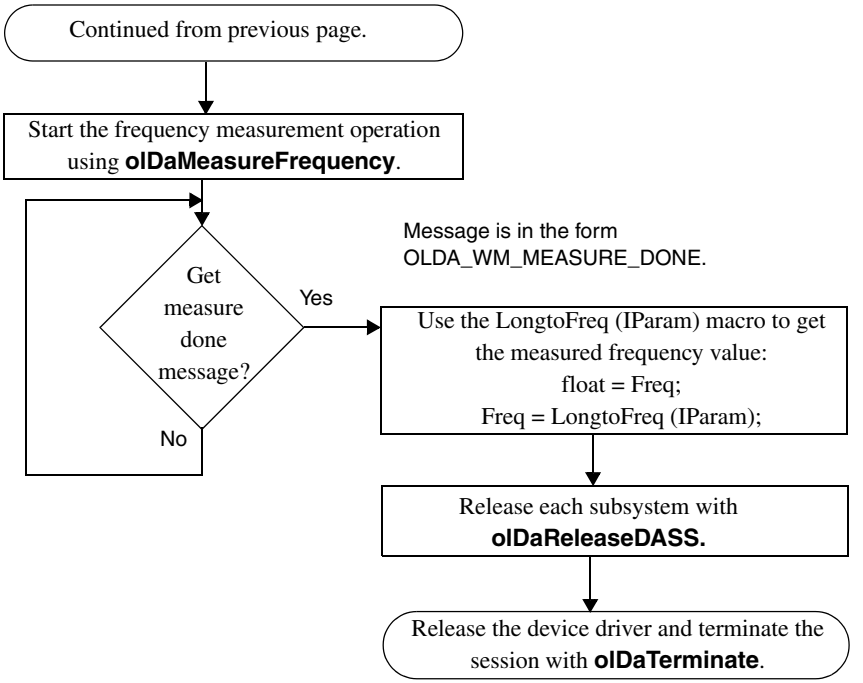
Frequency Measurement Operations

Note that this flowchart assumes that you are using the system timer to generate the period over which the frequency is measured. If you need more accuracy than the system timer provides, refer to page 54 in this manual and to the *DataAcq SDK User's Manual* for more information.

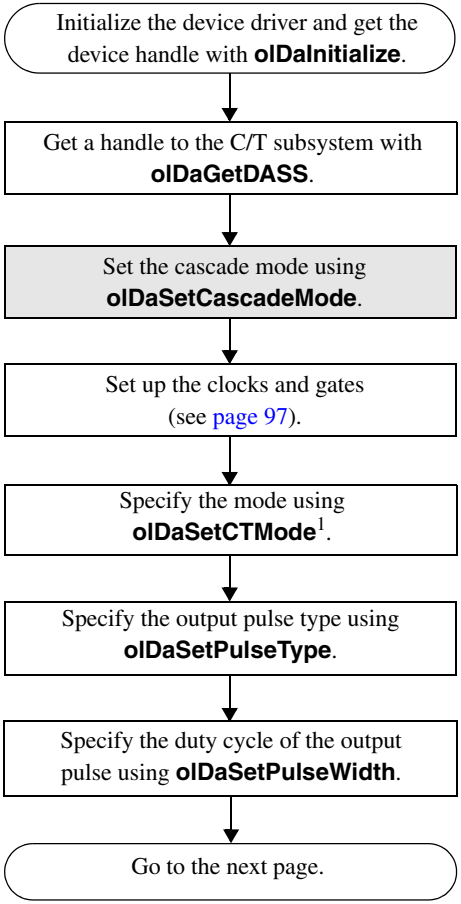

Initialize the device driver and get the device handle with **olDaInitialize**.
Get a handle to the C/T subsystem with **olDaGetDASS**.[1]
Set the cascade mode using **olDaSetCascadeMode**.
Set up the clocks (see page 97).
Specify the mode as OL_CTMODE_COUNT using **olDaSetCTMode**.
Configure the subsystem using **olDaConfig**.
Go to the next page.

[1] Specify the appropriate C/T subsystem/element. The Windows device driver supports two elements (0 and 1).

Frequency Measurement Operations (cont.)

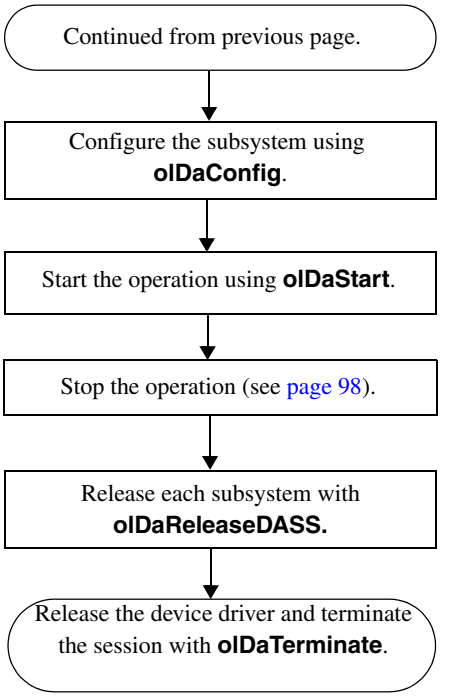

Continued from previous page.
Start the frequency measurement operation using **olDaMeasureFrequency**.
Get measure done message?
Yes
No
Message is in the form OLDA_WM_MEASURE_DONE.
Use the LongtoFreq (IParam) macro to get the measured frequency value:
float = Freq;
Freq = LongtoFreq (IParam);
Release each subsystem with **olDaReleaseDASS.**
Release the device driver and terminate the session with **olDaTerminate**.

Pulse Output Operations


Initialize the device driver and get the device handle with **olDaInitialize**.
Get a handle to the C/T subsystem with **olDaGetDASS**.
Set the cascade mode using **olDaSetCascadeMode**.
Set up the clocks and gates (see page 97).
Specify the mode using **olDaSetCTMode**[1].
Specify the output pulse type using **olDaSetPulseType**.
Specify the duty cycle of the output pulse using **olDaSetPulseWidth**.
Go to the next page.

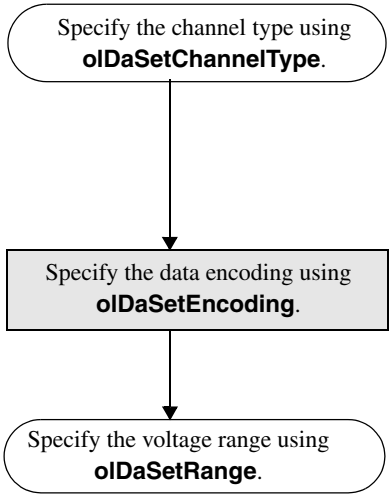
[1] Specify OL_CTMODE_RATE for rate generation (continuous pulse output), OL_CTMODE_ONESHOT for single one-shot, or OL_CTMODE_ONESHOT_RPT for repetitive one-shot.

Pulse Output Operations (cont.)


Continued from previous page.
Configure the subsystem using **olDaConfig**.
Start the operation using **olDaStart**.
Stop the operation (see page 98).
Release each subsystem with **olDaReleaseDASS.**
Release the device driver and terminate the session with **olDaTerminate**.

Note that this step is not needed for single one-shot operations.

Set Subsystem Parameters


Specify the channel type using **olDaSetChannelType**.
Specify the data encoding using **olDaSetEncoding**.
Specify the voltage range using **olDaSetRange**.

For A/D operations, specify the channel type as single-ended (for single-ended or pseudo-differential channels), or differential. For all other operations, specify differential (the default).

Specify the data encoding type as binary (OL_ENC_BINARY). This is the default value.

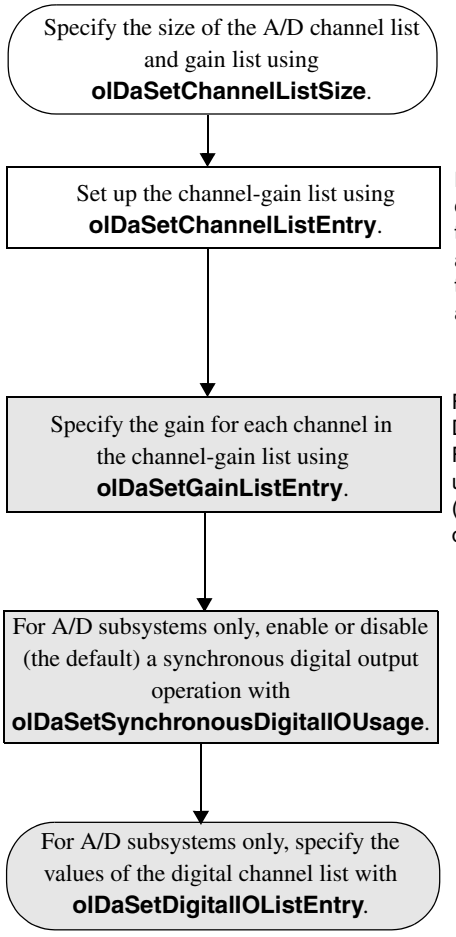
For the A/D subsystems on the DT9801, DT9801-MAC, DT9801-EC, DT9801-EC-I, DT9802, DT9802-MAC, DT9802-EC, and DT9802-EC-I, specify the voltage input range as 0 to 10 V or ±10 V (the default).

For the A/D subsystems on the DT9803, DT9803-MAC, DT9803-EC, DT9803-EC-I, DT9804, DT9804-MAC, DT9804-EC, DT9804-EC-I, DT9805, and DT9806, specify the voltage input range as ±10 V. The input range and the gain determine the effective input range. See page 19 for more information.

For D/A subsystems on the DT9802, DT9802-MAC, DT9802-EC, and DT9802-EC-I, specify the voltage output range as 0 to 10 V, 0 to 5 V, ±10 V (the default), or ±5 V. For D/A subsystems on the DT9804, DT9804-MAC, DT9804-EC, DT9804-EC-I, and DT9806, specify the voltage output range as ±10 V.

The step is unnecessary for DIN and DOUT subsystems.

Set Up Channel List and Channel Parameters


Specify the size of the A/D channel list and gain list using **olDaSetChannelListSize**.
Set up the channel-gain list using **olDaSetChannelListEntry**.
Specify the gain for each channel in the channel-gain list using **olDaSetGainListEntry**.
For A/D subsystems only, enable or disable (the default) a synchronous digital output operation with **olDaSetSynchronousDigitalIOUsage**.
For A/D subsystems only, specify the values of the digital channel list with **olDaSetDigitalIOListEntry**.

The default is 1. The maximum size is 32.

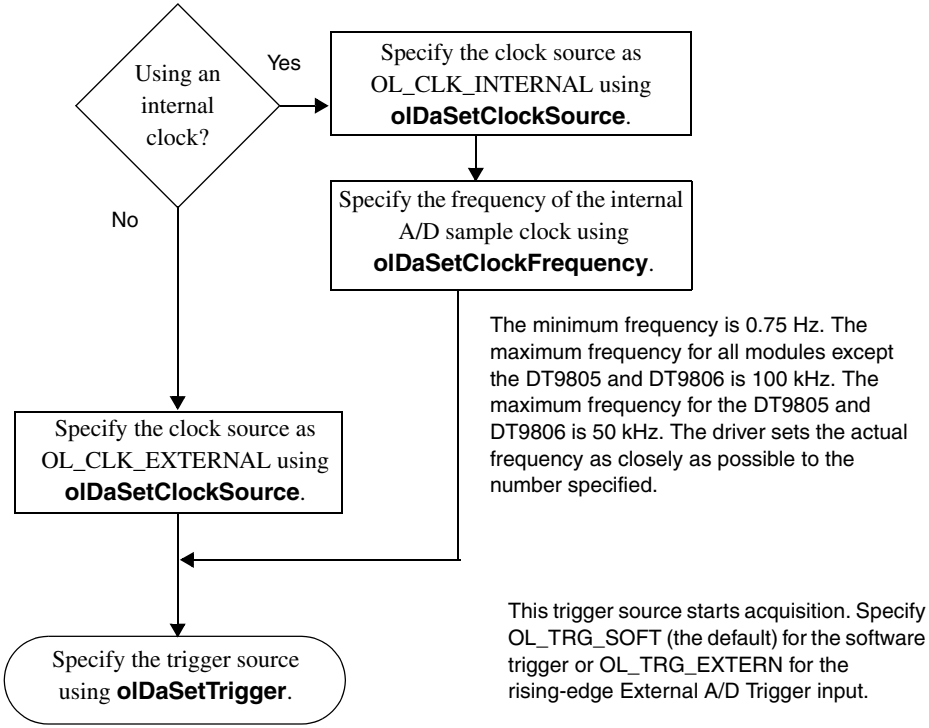
For the single-ended and pseudo-differential configuration, channels 0 to 15 are available; for the differential configuration, channels 0 to 7 are available. To achieve continuous digital input, enter the digital input channel as channel 16 in the analog input channel list.

For A/D operations on all modules except the DT9805 and DT9806, use a gain of 1, 2, 4, or 8. For A/D operations on the DT9805 and DT9806, use a gain of 1, 10, 100, or 500. Use a gain of 1 (the default) if you use digital channel 16 and for all other operations.

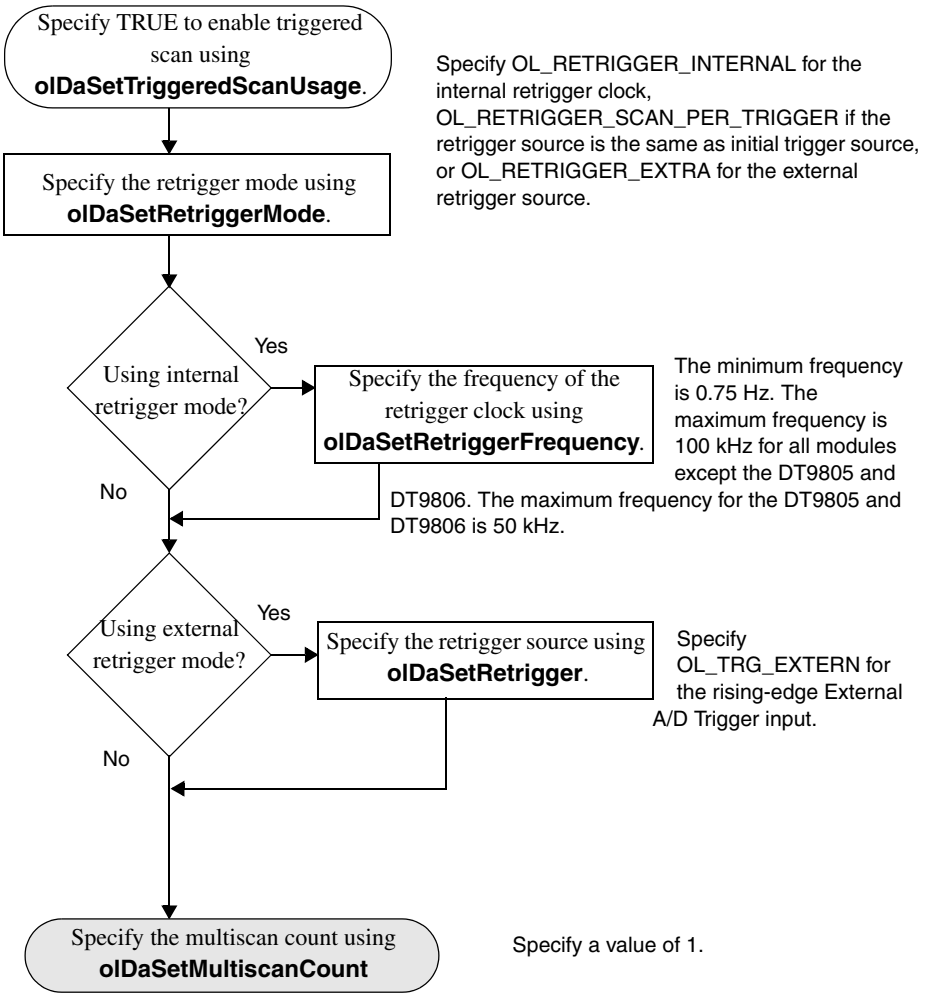
If you want to output data to the dynamic digital output line, enable synchronous digital output operation.

Values range from 0 (the default) to 1. As each entry of the analog channel list is sampled, the value of the corresponding entry in the digital list is output to the dynamic digital output line.

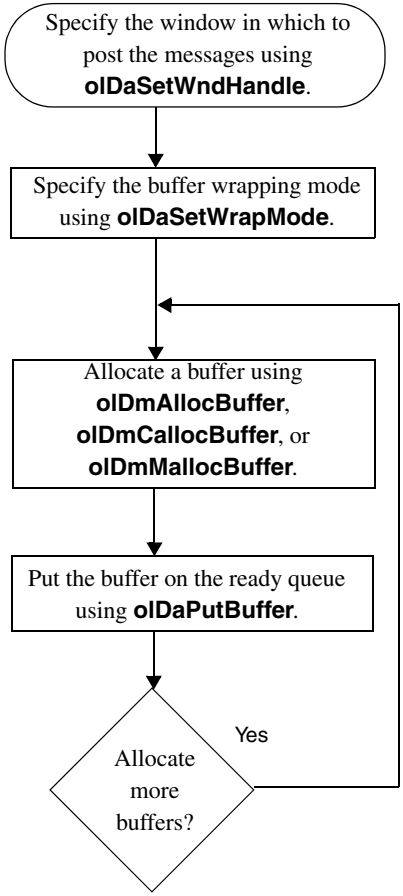
Set Clocks and Triggers


Using an internal clock?
Yes
No
Specify the clock source as OL_CLK_INTERNAL using **olDaSetClockSource**.
Specify the frequency of the internal A/D sample clock using **olDaSetClockFrequency**.
The minimum frequency is 0.75 Hz. The maximum frequency for all modules except the DT9805 and DT9806 is 100 kHz. The maximum frequency for the DT9805 and DT9806 is 50 kHz. The driver sets the actual frequency as closely as possible to the number specified.
Specify the clock source as OL_CLK_EXTERNAL using **olDaSetClockSource**.
Specify the trigger source using **olDaSetTrigger**.
This trigger source starts acquisition. Specify OL_TRG_SOFT (the default) for the software trigger or OL_TRG_EXTERN for the rising-edge External A/D Trigger input.

Set Up Triggered Scan


Specify TRUE to enable triggered scan using **olDaSetTriggeredScanUsage**.
Specify the retrigger mode using **olDaSetRetriggerMode**.
Specify OL_RETRIGGER_INTERNAL for the internal retrigger clock, OL_RETRIGGER_SCAN_PER_TRIGGER if the retrigger source is the same as initial trigger source, or OL_RETRIGGER_EXTRA for the external retrigger source.
Using internal retrigger mode?
Yes
No
Specify the frequency of the retrigger clock using **olDaSetRetriggerFrequency**.
The minimum frequency is 0.75 Hz. The maximum frequency is 100 kHz for all modules except the DT9805 and DT9806. The maximum frequency for the DT9805 and DT9806 is 50 kHz.
Using external retrigger mode?
Yes
No
Specify the retrigger source using **olDaSetRetrigger**.
Specify OL_TRG_EXTERN for the rising-edge External A/D Trigger input.
Specify the multiscan count using **olDaSetMultiscanCount**
Specify a value of 1.

Set Up A/D Buffering

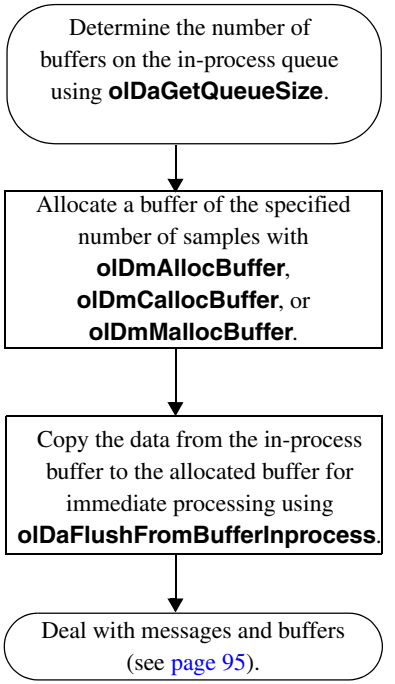

Specify the window in which to post the messages using **olDaSetWndHandle**.
Specify the buffer wrapping mode using **olDaSetWrapMode**.
Allocate a buffer using **olDmAllocBuffer**, **olDmCallocBuffer**, or **olDmMallocBuffer**.
Put the buffer on the ready queue using **olDaPutBuffer**.
Allocate more buffers?
Yes

Specify OL_WRP_NONE if buffers are not reused, OL_WRP_MULTIPLE if buffers are continuously reused when none are found on the ready queue, or OL_WRP_SINGLE if one buffer is continuously reused.

Specify a buffer size at least as large as the sampling rate; for example, if you are using a sampling rate of 100 kSamples/s (100 kHz), specify a buffer size of 100,000. The minimum buffer size that you should specify is 256 samples.

A minimum of three buffers is recommended.

Transfer Data from an In-process Buffer

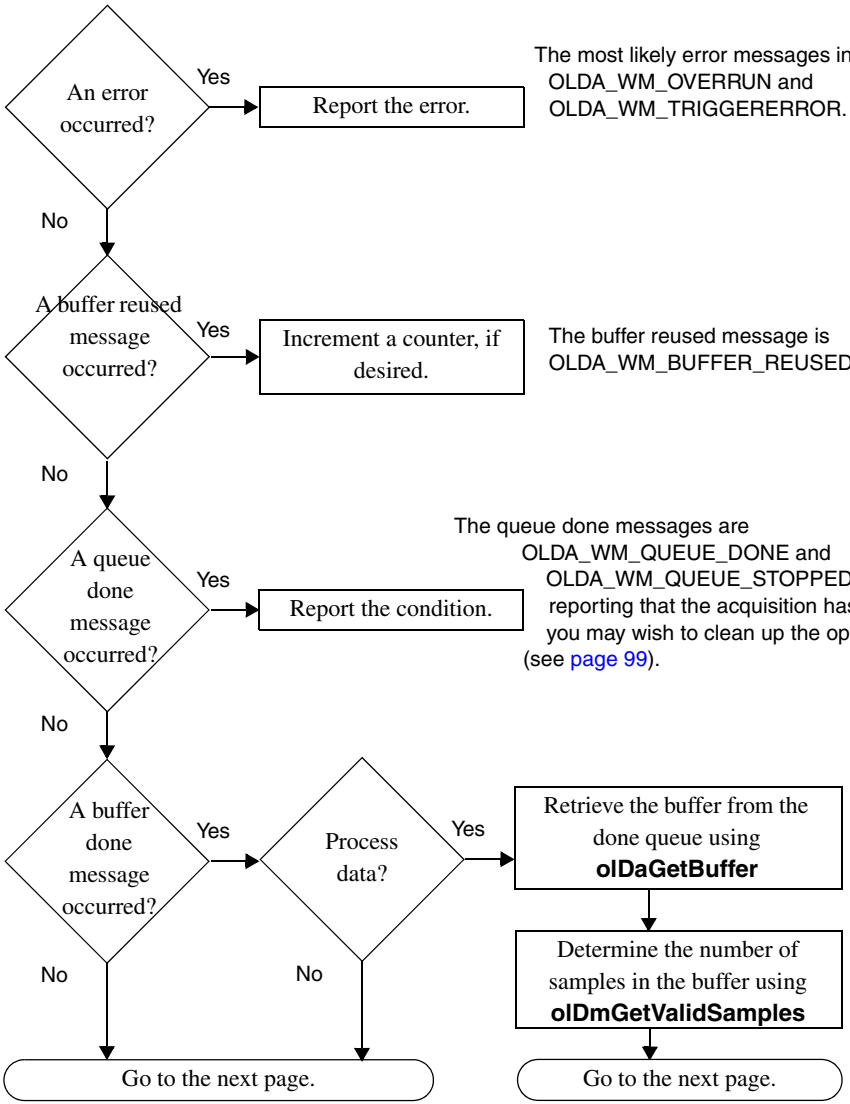

Determine the number of buffers on the in-process queue using **olDaGetQueueSize**.
Allocate a buffer of the specified number of samples with **olDmAllocBuffer**, **olDmCallocBuffer**, or **olDmMallocBuffer**.
Copy the data from the in-process buffer to the allocated buffer for immediate processing using **olDaFlushFromBufferInprocess**.
Deal with messages and buffers (see page 95).

At least one must exist.

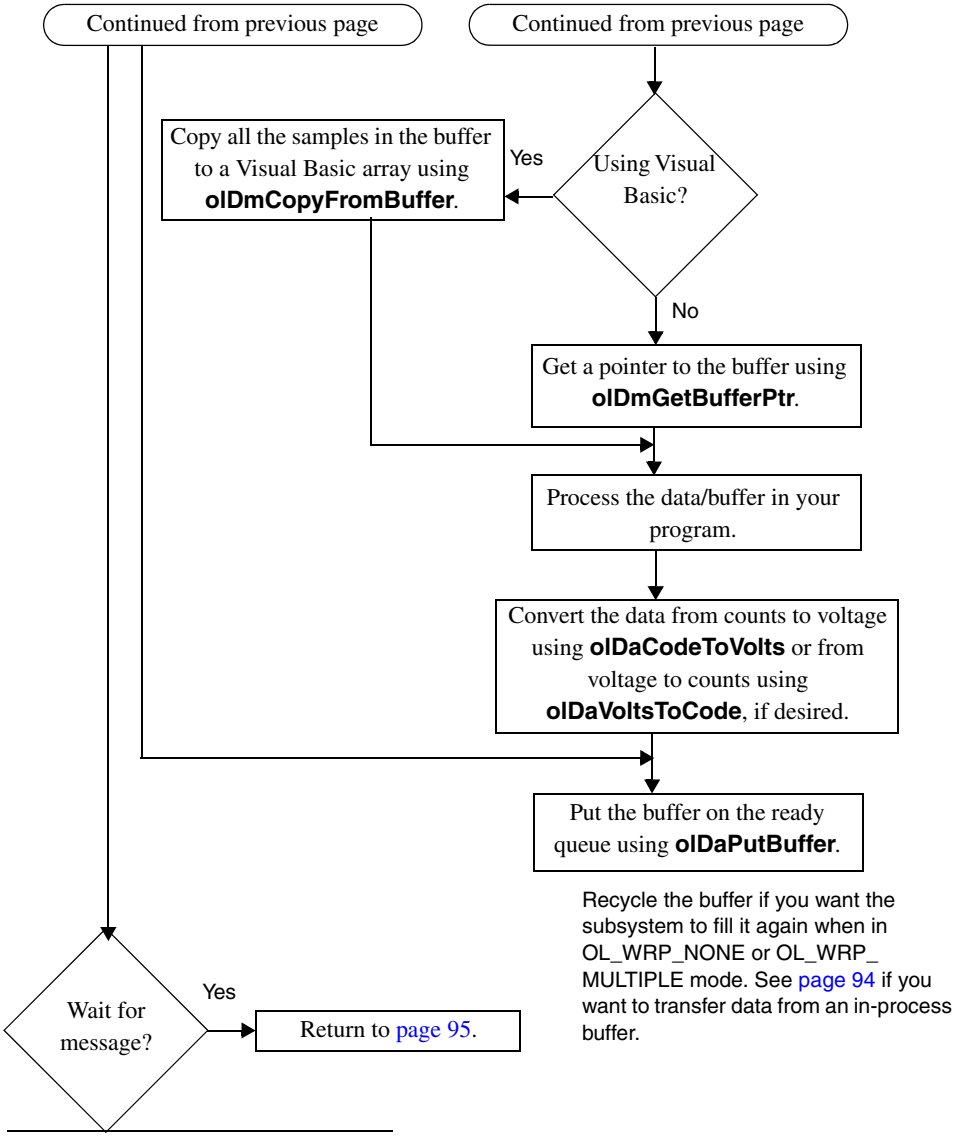
The buffer into which in-process data was copied was put onto the done queue by the driver, resulting in an OLDA_WM_BUFFER_ DONE message.

When the in-process buffer has been filled, it too is placed on the done queue and an OLDA_WM_BUFFER_DONE message is posted. However, the number of valid samples is equal to the queue's maximum samples minus what was copied out.

Deal with A/D Messages and Buffers

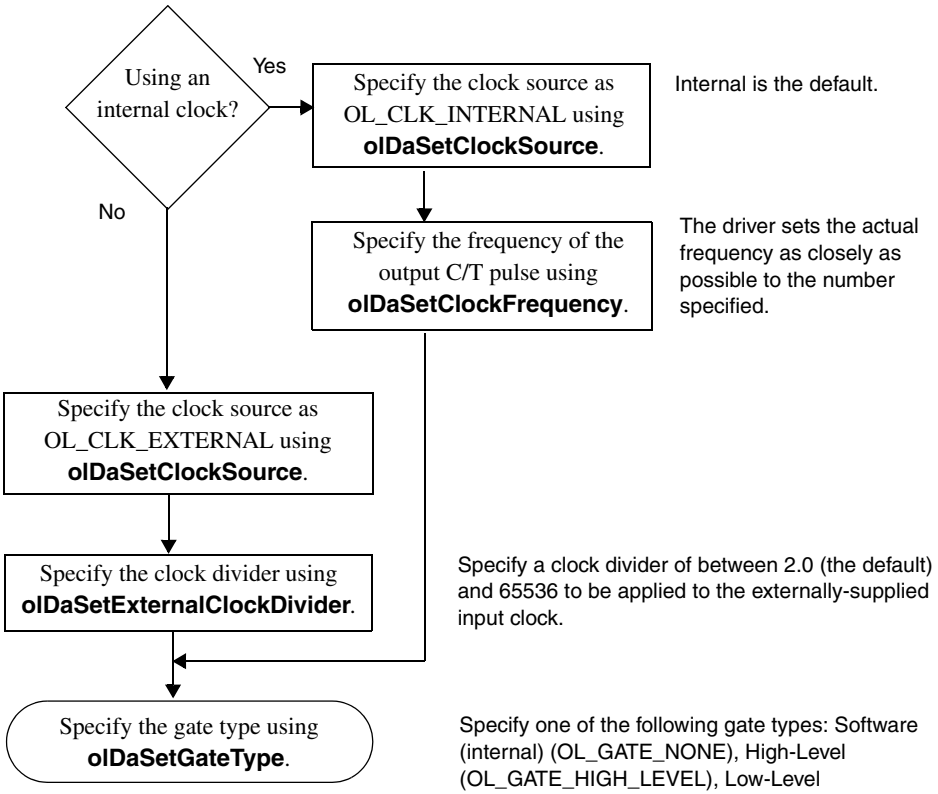

An error occurred?
Yes
Report the error.
The most likely error messages include OLDA_WM_OVERRUN and OLDA_WM_TRIGGERERROR.
No
A buffer reused message occurred?
Yes
Increment a counter, if desired.
The buffer reused message is OLDA_WM_BUFFER_REUSED.
No
A queue done message occurred?
Yes
Report the condition.
The queue done messages are OLDA_WM_QUEUE_DONE and OLDA_WM_QUEUE_STOPPED. After reporting that the acquisition has stopped, you may wish to clean up the operation (see page 99).
No
A buffer done message occurred?
Yes
Process data?
Yes
Retrieve the buffer from the done queue using olDaGetBuffer
Determine the number of samples in the buffer using olDmGetValidSamples
No
No
Go to the next page.
Go to the next page.

Deal with A/D Messages and Buffers (cont.)

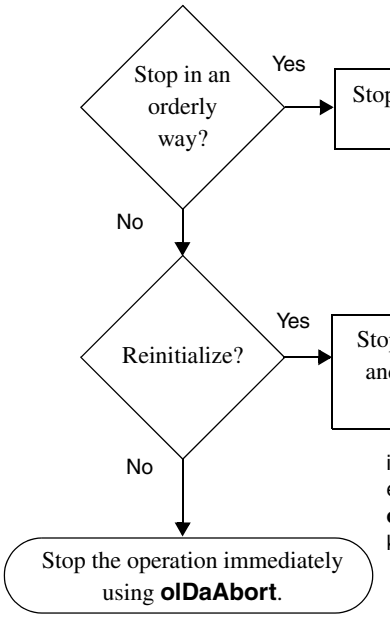

Continued from previous page
Continued from previous page
Using Visual Basic?
Yes
Copy all the samples in the buffer to a Visual Basic array using **olDmCopyFromBuffer**.
No
Get a pointer to the buffer using **olDmGetBufferPtr**.
Process the data/buffer in your program.
Convert the data from counts to voltage using **olDaCodeToVolts** or from voltage to counts using **olDaVoltsToCode**, if desired.
Put the buffer on the ready queue using **olDaPutBuffer**.
Recycle the buffer if you want the subsystem to fill it again when in OL_WRP_NONE or OL_WRP_MULTIPLE mode. See page 94 if you want to transfer data from an in-process buffer.
Wait for message?
Yes
Return to page 95.

[1] The buffer done message is OLDA_WM_BUFFER_DONE or OLDA_WM_PRETRIGGER_BUFFER_DONE.

Set Clocks and Gates for Counter/Timer Operations


Using an internal clock?
Yes
No
Specify the clock source as OL_CLK_INTERNAL using **olDaSetClockSource**.
Internal is the default.
Specify the frequency of the output C/T pulse using **olDaSetClockFrequency**.
The driver sets the actual frequency as closely as possible to the number specified.
Specify the clock source as OL_CLK_EXTERNAL using **olDaSetClockSource**.
Specify the clock divider using **olDaSetExternalClockDivider**.
Specify a clock divider of between 2.0 (the default) and 65536 to be applied to the externally-supplied input clock.
Specify the gate type using **olDaSetGateType**.
Specify one of the following gate types: Software (internal) (OL_GATE_NONE), High-Level (OL_GATE_HIGH_LEVEL), Low-Level (OL_GATE_LOW_LEVEL), High-Edge (OL_GATE_HIGH_EDGE) or Low-Edge (OL_GATE_LOW_EDGE).

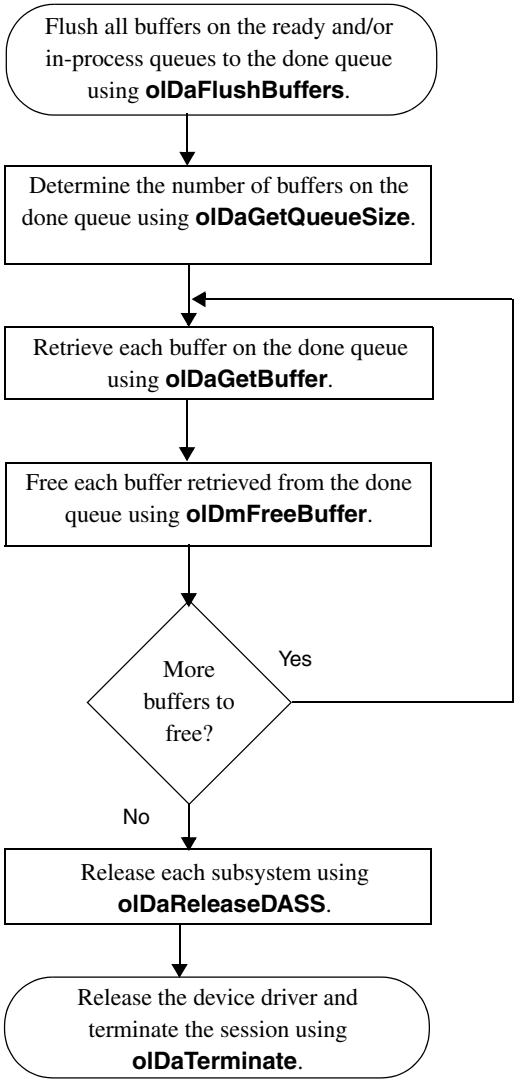
Stop the Operation



olDaStop stops the operation on the subsystem in the orderly way; the current in-process buffers are filled or emptied and put on the done queue. The driver posts at least one buffer done and queue stopped message.

olDaAbort and **olDaReset** stop the operation on the subsystem immediately; the current buffers are not filled or emptied before they are put on the done queue. **olDaReset** also reinitializes the subsystem to a known state and flushes all buffers to the done queue.

Clean up the Operation


Flush all buffers on the ready and/or in-process queues to the done queue using **olDaFlushBuffers**.
Determine the number of buffers on the done queue using **olDaGetQueueSize**.
Retrieve each buffer on the done queue using **olDaGetBuffer**.
Free each buffer retrieved from the done queue using **olDmFreeBuffer**.
More buffers to free?
Yes
No
Release each subsystem using **olDaReleaseDASS**.
Release the device driver and terminate the session using **olDaTerminate**.

Calibration

Running the Calibration Utility 103
Calibrating the Analog Input Subsystem 104

Note: The DT9800 Series Calibration Utility is provided for Windows 98, Windows Me, Windows 2000, and Windows XP only.

The DT9800 Series function modules are calibrated at the factory and should not require calibration for initial use. It is recommended that you check and, if necessary, readjust the calibration of the analog I/O circuitry on the DT9800 Series function modules every six months.

Note: Ensure that you installed the DT9800 Series software and configured the device driver prior to using the DT9800 Series Calibration Utility. Refer to the *DT9800 Series Getting Started Manual* for more information.

This chapter describes how to run the DT9800 Series Calibration Utility and calibrate the analog I/O circuitry of the DT9800 Series function modules.

Running the Calibration Utility

To run the DT9800 Series Calibration Utility, perform the following step:

1. Locate the DT9800 Series software program folder on your hard disk.
   This program folder was created when you installed the DT9800 Series software.
2. Double-click the **Calibration Utility** icon in the program folder.
3. Select the name of the DT9800 Series function module to configure from the combo box, then click **OK**.

Once the DT9800 Series Calibration Utility is running, you can calibrate the analog I/O circuitry, as described in the following subsections.

Calibrating the Analog Input Subsystem

The following sections describe how to configure your module for calibration and how to calibrate the analog input circuitry of your module.

Configuring for Calibration

To calibrate the analog input circuitry, use an external +9.3750 V precision voltage source available from vendors such as Electronic Development Corporation (EDC). Using an external +9.3750 V precision voltage source provides an accuracy of approximately ±1 LSB for DT9801, DT9801-EC, DT9801-EC-I, DT9802, DT9802-EC, and DT9802-EC-I function modules and ±3 LSBs for the DT9803, DT9803-EC, DT9803-EC-I, DT9804, DT9804-EC, DT9804-EC-I, DT9805, and DT9806 function modules.

Perform the following steps to configure a DT9800 Series function module for calibration:

1. Connect Analog Input 0 (TB1) to the positive side of the precision voltage source.
2. Connect Analog Input 0 Return (TB2) to the negative side of the precision voltage source.
3. Connect Analog Input 0 Return (TB2) to Analog Ground (TB17).
4. Connect Analog In 1 (TB3) to Analog In 1 Return (TB4) and to Analog Ground (TB17).

When you are finished connecting the external reference, calibrate the module, as described in the next section.

Calibrating the Analog Input Circuitry

You can choose to calibrate the analog input circuitry automatically (described on this page) or manually (described on page 106); auto-calibration is the easiest to use and is the recommended calibration method.

Using the Auto-Calibration Procedure

To calibrate the analog input subsystem automatically, perform the following step:

1. Click **Go** in the Auto Calibration box.
   The zero and full-scale ranges are automatically calibrated.

Note: If you are not satisfied with the analog input calibration, you can load the factory default settings stored in the EEPROM by clicking **Restore** in the A/D Configuration Factory Settings box.

Once you have finished this procedure, the analog input circuitry is calibrated. If you are using a DT9805 or DT9806 function module, it is recommended that you calibrate the thermocouple circuitry using the instructions on page 107. Otherwise, you can calibrate the analog output circuitry, if you wish, following the instructions on page 109.

Using the Manual Calibration Procedure

To calibrate the analog input subsystem manually, perform the following steps:

1. Click **A/D Ch. 1**.
2. Click the increment or decrement arrows in the Offset box until the A/D value on the screen reads 0 V (within 0.001 V for the DT9803, DT9803-EC, DT9803-EC-I, DT9804, DT9804-EC, DT9804-EC-I, DT9805, and DT9806 modules and within 0.010 V for the DT9801, DT9801-EC, DT9801-EC, DT9802, DT9802-EC, and DT9802-EC-I modules).
3. Click **A/D Ch. 0**.
4. Click the increment or decrement arrows in the Gain box until the A/D value on the screen reads +9.3750 V (within 0.001 V for the DT9803, DT9803-EC, DT9803-EC-I, DT9804, DT9804-EC, DT9804-EC-I, DT9805, and DT9806 modules and within 0.010 V for the DT9801, DT9801-EC, DT9801-EC-I, DT9802, DT9802-EC, and DT9802-EC-I modules).

Note: If you are not satisfied with the analog input calibration, you can load the factory default settings stored in the EEPROM by clicking **Restore** in the A/D Configuration Factory Settings box.

Once you have finished this procedure, the analog input circuitry is calibrated. If you are using a DT9805 or DT9806 function module, it is recommended that you calibrate the thermocouple circuitry using the instructions in the next section. Otherwise, you can calibrate the analog output circuitry, if you wish, following the instructions on page 109.

Calibrating the Thermocouple Circuitry

Note: Ensure that the DT9805 or DT9806 module has been running for about 1/2 hour (allowing the module to warm up) and that you have calibrated the analog input circuitry using the procedure described on page 104 before calibrating the thermocouple circuitry.

To calibrate the thermocouple circuitry on the DT9805 or DT9806 modules, perform the following steps:

1. Disconnect all signals to Analog Input 0 (TB1), leaving it open (no connections).
2. Connect Analog In 1 (TB3) to Analog In 1 Return (TB4) and to Analog Ground (TB17).
3. In the PGL Zero box, click the text **A/D Gain=500, CH 1** to refresh the value of analog input channel 1.
   The gain is set to 500 automatically.
4. Click the increment or decrement arrows in the PGL Zero box until the A/D value reads 0 V (within 5 mV).
5. Measure the room temperature at the temperature sensor of the board (see Figure 15) by taping a thermometer to the underside of the module between screw terminals 9 and 10, then multiply this value by 10 mV.
   This is the temperature that you want to adjust the CJC to.

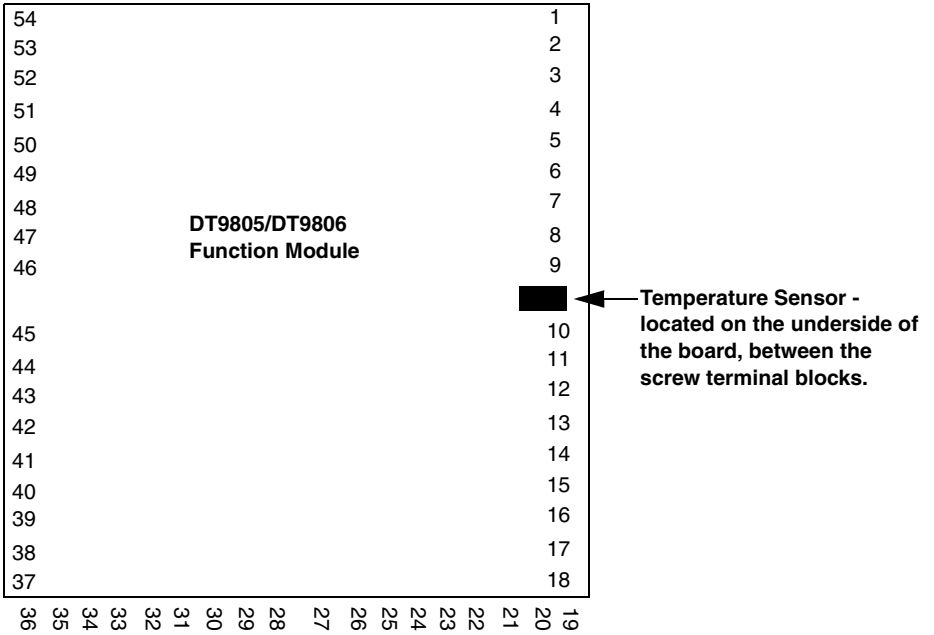


Figure 15: Temperature Sensor Location

6. Click the text **A/D Gain=1, CH 0** in the CJC Adj. box to refresh the value of analog input channel 0.
   The gain is set to 1 automatically.
7. Click the increment or decrement arrows in the CJC Adj. box until the A/D value on the screen is equal to the room temperature multiplied by 10 mV (within 5 mV). For example, if the room temperature is 25° C, you want to adjust the CJC to 250 mV (within 5 mV).

Note: If you are not satisfied with the thermocouple calibration, you can load the factory default settings stored in the EEPROM by clicking **Restore** in the Thermocouple Calibration Factory Settings box.

Once you have finished this procedure, the thermocouple circuitry is calibrated. You can now calibrate the analog output circuitry, if you wish, following the instructions in the next section.

Calibrating the Analog Output Subsystem

To calibrate the analog output circuitry of the DT9802, DT9802-EC, DT9802-EC-I, DT9804, DT9804-EC, DT9804-EC-I, or DT9806 modules, use an external precision meter available from vendors such as Fluke.

To calibrate the analog output circuitry, perform the following steps:

1. Connect Analog Output 0+ (TB19) to the positive side of the precision voltage meter.
2. Connect Analog Output 0 Return (TB20) to the negative side of the precision voltage meter.
3. In the DAC0 Voltage box, click **0.000 V**.
4. In the DAC0 Adjustment box, click the increment or decrement arrows until your external meter display reads 0 V (within 0.005 V).
5. In the DAC0 Voltage box, click **+9.375 V** and verify that your external meter display reads +9.375 V (within ±12 mV.)
6. Connect Analog Output 1+ (TB21) to the positive side of the precision voltage meter.
7. Connect Analog Output 1 Return (TB22) to the negative side of the precision voltage meter.

8. In the DAC1 Voltage box, click **0.000 V**.
9. In the DAC1 Adjustment box, click the increment or decrement arrows until your external meter display reads 0 V (within 0.005 V).
10. In the DAC1 Voltage box, click **+9.375 V** and verify that your external meter display reads +9.375 V (within ±12 mV.)

Note: If you are not satisfied with the analog output calibration, you can load the factory default settings stored in the EEPROM by clicking **Restore** in the D/A Calibration Factory Settings box.

Once you have finished this procedure, the analog output circuitry is calibrated.

To close the Calibration Utility, click **Done**.

Troubleshooting

General Checklist 112
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General Checklist

Should you experience problems using the DT9800 Series function modules, please follow these steps:

1. Read all the documentation provided for your product. Make sure that you have added any "Read This First" information to your manual and that you have used this information.
2. Check the Data Acquisition OMNI CD for any README files and ensure that you have used the latest installation and configuration information available.
3. Check that your system meets the requirements stated in the *DT9800 Series Getting Started Manual*.
4. Check that you have installed your hardware properly using the instructions in the *DT9800 Series Getting Started Manual*.
5. Check that you have installed and configured the device driver properly using the instructions in the *DT9800 Series Getting Started Manual*.
6. Search the DT Knowledgebase in the Support section of the Data Translation web site (at www.datatranslation.com) for an answer to your problem.

If you still experience problems, try using the information in Table 14 to isolate and solve the problem. If you cannot identify the problem, refer to page 113.

Table 14: Troubleshooting Problems

Symptom	Possible Cause	Possible Solution
Module does not respond.	The module configuration is incorrect.	Check the configuration of your device driver; see the instructions in the *DT9800 Series Getting Started Manual*.
	The module is damaged.	Contact Data Translation for technical support; refer to page 115.
Intermittent operation.	Loose connections or vibrations exist.	Check your wiring and tighten any loose connections or cushion vibration sources; see the instructions in the *DT9800 Series Getting Started Manual*.
	The module is overheating.	Check environmental and ambient temperature; consult the module's specifications on page 129 of this manual and the documentation provided by your computer manufacturer for more information.
	Electrical noise exists.	Check your wiring and either provide better shielding or reroute unshielded wiring; see the instructions in the *DT9800 Series Getting Started Manual*.

Table 14: Troubleshooting Problems (cont.)

Symptom	Possible Cause	Possible Solution
Device failure error reported.	The DT9800 Series function module cannot communicate with the Microsoft bus driver or a problem with the bus driver exists.	Check your cabling and wiring and tighten any loose connections; see the instructions in the *DT9800 Series Getting Started Manual*.
	The DT9800 Series function module was removed while an operation was being performed.	Ensure that your DT9800 Series function module is properly connected; see the instructions in the *DT9800 Series Getting Started Manual*.
Data appears to be invalid.	An open connection exists.	Check your wiring and fix any open connections; see the instructions in the *DT9800 Series Getting Started Manual*.
	A transducer is not connected to the channel being read.	Check the transducer connections; see the instructions in the *DT9800 Series Getting Started Manual*.
	The module is set up for differential inputs while the transducers are wired as single-ended inputs or vice versa.	Check your wiring and ensure that what you specify in software matches your hardware configuration; see the instructions in the *DT9800 Series Getting Started Manual*.
Computer does not boot.	The power supply of the computer is too small to handle all the system resources.	Check the power requirements of your system resources and, if needed, get a larger power supply; consult the module's specifications on page 129 of this manual.

Service and Support

If you have difficulty using the DT9841 module, Data Translation's Technical Support Department is available to provide technical assistance.

Telephone Technical Support

For the most efficient service, complete the form on page 116 and be at your computer when you call for technical support. This information helps to identify specific system and configuration-related problems and to replicate the problem in house, if necessary.

You can reach the Technical Support Department by calling (508) 481-3700 x1001. If you are located outside the USA, call your local distributor. The name and telephone number of you nearest distributor are provided in your Data Translation catalog.

If you are leaving a message to request a support call, please include the following information:

- Your name (please include proper spelling),
- Your company or organization (please include proper spelling),
- A phone number,
- An email address where you can be reached,
- The hardware/software product you need help on,
- A summary of the issue or question you have,
- Your contract number, if applicable, and
- Your product serial number or purchase date.

Omitting any of the above information may delay our ability to resolve your issue.

Information Required for Technical Support

Name:_____Phone_____
Contract Number: _____
Address: _____
_____

Data Translation hardware product(s): _____
serial number: _____
configuration: _____
Data Translation device driver - SPO number: _____ _____
_____ version: _____
Data Translation software - SPO number:_____ _____
serial number: _____ version:_____
PC make/model: _____
operating system: _____ version:_____
Windows version: _____
processor: _____ speed:_____
RAM: _____ hard disk space:_____
network/number of users: _____ disk cache:_____
graphics adapter: _____ data bus:_____

I have the following boards and applications installed in my system:_____
_____
_____
I am encountering the following problem(s): _____
_____
_____
_____
and have received the following error messages/codes: _____
_____
_____
I have run the board diagnostics with the following results: _____
_____
You can reproduce the problem by performing these steps:
1. _____
_____
2. _____
_____
3. _____
_____

E-Mail and Fax Support

You can also get technical support by e-mailing or faxing the Technical Support Department:

- **E-mail**: You can reach Technical Support at the following address: tsupport@datx.com

  Ensure that you provide the following minimum information:

  – Your name,

  – Your company or organization,

  – A phone number,

  – An e-mail address where you can be reached,

  – The hardware/software product you need help on,

  – A summary of the issue you are experiencing,

  – Your contract number, if applicable, and

  – Your product serial number or purchase date.

  Omitting any of the above information may delay the resolution of your issue.

- **Fax**: Photocopy and complete the form on page 116, then fax Technical Support at the following number: (508) 481-8620.

World-Wide Web Support

For the latest tips, software fixes, and other product information, you can always access our World-Wide Web site free of charge at the following address: http://www.datatranslation.com

If Your Board Needs Factory Service

If your board must be returned to Data Translation, perform the following steps:

1. Record the board's serial number, then contact the Customer Service Department at (508) 481-3700 (if you are in the USA) and obtain a Return Material Authorization (RMA).

   If you are located outside the USA, call your local distributor for authorization and shipping instructions. The name and telephone number of your nearest distributor are listed in your Data Translation catalog. All return shipments to Data Translation must be marked with the correct RMA number to ensure proper processing.

2. Using the original packing materials, if available, package the board as follows:

   – Wrap the board in an electrically conductive plastic material. Handle with ground protection. A static discharge can destroy components on the board.

   – Place in a secure shipping container.

3. Return the board to the following address, making sure the RMA number is visible on the outside of the box.

   Customer Service Dept.
   Data Translation, Inc.
   100 Locke Drive
   Marlboro, MA 01752-1192

Specifications

Table 15 lists the specifications for the A/D subsystem.

Table 15: A/D Subsystem Specifications

Feature	DT9801/-MAC/-EC/-EC-I, DT9802/-MAC/-EC/-EC-I Specifications	DT9803/-MAC/-EC/-EC-I, DT9804/-MAC/-EC/-EC-I, DT9805, DT9806 Specifications
Number of analog inputs Single-ended/ pseudo-differential: Differential:	16 8	
Number of gains	4 (1, 2, 4, 8)	4 (1, 2, 4, and 8 for DT9803/04; 1, 10, 100, 500 for DT9805/06)
Resolution	12 bits	16 bits
Data encoding	Offset binary	
Coupling	DC	
Over voltage protection Off: On:	±40 V ±25 V	
ESD protection	1.5 kV	
System Error	0.03% FSR	0.01% FSR

Table 15: A/D Subsystem Specifications (cont.)

Feature	DT9801/-MAC/-EC/-EC-I, DT9802/-MAC/-EC/-EC-I Specifications	DT9803/-MAC/-EC/-EC-I, DT9804/-MAC/-EC/-EC-I, DT9805, DT9806 Specifications
System accuracy (full-scale) Gain = 1: Gain = 2: Gain = 4: Gain = 8: (DT9805/9806 only) Gain = 10: Gain = 100: Gain = 500:	 0.03% 0.04% 0.05% 0.05%	 0.01% 0.02% 0.03% 0.03% 0.02% 0.03% 0.04%
Nonlinearity (integral)	±1.0 LSBs	±4.0 LSBs
Differential linearity	±0.5 LSBs (no missing codes)	±1.0 LSBs (no missing codes) for DT9803/04 ±1.2 LSBs (no missing codes) for DT9805/06
Range	0 to 1.25 V, 2.5 V, 5 V, 10 V ±1.25, 2.5, 5, 10 V	±1.25 V, 2.5 V, 5 V, 10 V for DT9803/04 ±0.020 V, 0.10 V, 1 V, 10 V for DT9805/06
Drift Zero: Gain:	 ±30 µV+ (+20 µV * Gain)/° C ±30 ppm/° C	 ±25 µV+ (+10 µV * Gain)/° C for DT9803/04 ±25 µV+ (+5 µV * Gain)/° C for DT9805/06 ±20 ppm/° C

Table 15: A/D Subsystem Specifications (cont.)

Feature	DT9801/-MAC/-EC/-EC-I, DT9802/-MAC/-EC/-EC-I Specifications	DT9803/-MAC/-EC/-EC-I, DT9804/-MAC/-EC/-EC-I, DT9805, DT9806 Specifications
Input impedance Off: On:	100 MΩ, 10 pF[a] 100 MΩ, 100 pF[a]	
Channel-gain list	32 Samples	
Internal reference	+2.5 V ±0.002 V	
Input bias current	±20 nA	±20 nA for DT9803/04 ±10 nA for DT9805/06
Common mode voltage	±11 V maximum (operational)	
Maximum input voltage	±40 V maximum (protection)	
A/D converter noise	0.3 LSB rms	0.4 LSB rms
Amplifier input noise	20 μV rms + (10 μV rms * gain) 200 pA rms (current)	15 μV rms + (10 μV rms * gain) 100 pA rms (current)
Channel-to-channel offset	±40 μV	±40 μV
Channel acquisition time	3 μs	5 μs for DT9803/04 6 μs (Gain = 1) for DT9805/06 250 μs (Gain = 500) for DT9805/06
A/D conversion time	6.6 μs	8 μs

Table 15: A/D Subsystem Specifications (cont.)

Feature	DT9801/-MAC/-EC/-EC-I, DT9802/-MAC/-EC/-EC-I Specifications	DT9803/-MAC/-EC/-EC-I, DT9804/-MAC/-EC/-EC-I, DT9805, DT9806 Specifications
Effective number of bits (ENOB) at 1 kHz input	11.5 bits	13.5 bits for DT9803/04 14.1 bits for DT9805/06
Total Harmonic Distortion	-80 dB typical	-90 dB typical
Channel crosstalk	-80 dB @ 1 kHz	
Minimum Data Throughput (Internal Clock)	0.75 S/s	
Data throughput		
Single analog channel:	100 kSamples/s (0.03% accuracy)	100 kSamples/s for DT9803/04 (0.01% accuracy); 50 kSamples/s for DT9805/06 (0.01% accuracy)
Multiple channels (scan with gain of 1 to 10):	100 kSamples/s (0.03% accuracy)	100 kSamples/s for DT9803/04 (0.01% accuracy); 50 kSamples/s for DT9805/06 (0.01% accuracy)
Multiple channels (scan with gain of 100):	–	10 kSamples/s (0.03% accuracy)

Table 15: A/D Subsystem Specifications (cont.)

Feature	DT9801/-MAC/-EC/-EC-I, DT9802/-MAC/-EC/-EC-I Specifications	DT9803/-MAC/-EC/-EC-I, DT9804/-MAC/-EC/-EC-I, DT9805, DT9806 Specifications
Data throughput (cont.) Multiple channels (scan with gain of 500): Single digital channel:	– 100 kSamples/s	2 kSamples/s (0.04% accuracy) 100 kSamples/s for DT9803/04; 50 kSamples/s for DT9805/06
CJC Voltage @ 25° C	–	+0.250 V
Cold Junction Accuracy	–	+1° from 5° to 45° C
Break Detection Current[b]	–	+50 nA (high side differential)
External A/D sample clock Input type High-level input voltage: Low-level input voltage: Minimum pulse width: Maximum frequency:	 HCT Rising-Edge Sensitive with 22 kΩ pull-up resistor 2.4 V minimum 0.8 V maximum 600 ns (high); 600 ns (low) 750.0 kHz	

Table 15: A/D Subsystem Specifications (cont.)

Feature	DT9801/-MAC/-EC/-EC-I, DT9802/-MAC/-EC/-EC-I Specifications	DT9803/-MAC/-EC/-EC-I, DT9804/-MAC/-EC/-EC-I, DT9805, DT9806 Specifications
External A/D digital (TTL) trigger		
Input type	HCT Rising-Edge Sensitive with 22 kΩ pull-up resistor	
High-level input voltage:	2.4 V minimum	
Low-level input voltage:	0.8 V maximum	
Minimum pulse width:	600 ns (high); 600 ns (low)	
Maximum frequency:	750.0 kHz	
Dynamic Digital Output		
Output driver:	TTL	
Output driver high voltage:	2.4 V maximum (IOH = 1 mA)	
Output driver low voltage:	0.5 V maximum (IOL = 2 mA)	
Back EMF Diodes	Yes	

a. On channel 0 only on the DT9805 and DT9806 modules, the input impedance is 10 kΩ

b. Broken thermocouples in differential mode will output plus full scale for gains equal to or greater than 10.

Table 16 lists the specifications for the D/A subsystem.

Table 16: D/A Subsystem Specifications

Feature	DT9802/-MAC/-EC/-EC-I Specifications	DT9804/-MAC/-EC/-EC-I, DT9806 Specifications
Number of analog output channels	2	
Resolution	12 bits	16 bits
Data encoding (input)	Offset binary	
Nonlinearity (integral)	±1 LSBs	±4 LSBs
Differential linearity	±0.5 LSBs (monotonic)	±1.0 LSB (monotonic)
Output range	0 to 5 V, 10 V ±5 V, 10 V	±10 V
Zero error	Software-adjustable to zero	
Gain error	±2 LSBs	±6 LSBs
Current output	±5 mA minimum (10 V/ 2 kΩ)	
Output impedance	0.3 Ω typical	
Capacitive drive capability	0.001 µF minimum (no oscillations)	
Protection	Short circuit to Analog Common	
Power-on voltage	0 V ±10 mV maximum	
Settling time to 0.01% of FSR	50 µs, 20 V step; 10 µs, 100 mV step	
Throughput (Full Scale)	Single value (system dependent)	
Slew rate	2 V/µs	

Table 17 lists the specifications for the digital input subsystem.

Table 17: DIN Subsystem Specifications

Feature	Specifications
Number of lines	8 (Port A)
Termination	None
Inputs Input type: Input load: High-level input voltage: Low-level input voltage: High-level input current: Low-level input current:	 Level sensitive 1 (HCT) 2.0 V minimum 0.8 V maximum 3 µA -3 µA
Maximum internal pacer rate (single digital channel)[a]	Maximum A/D throughput of the board
Back EMF diodes	No

a. This digital channel must be the only channel included as part of the channel-gain list.

Table 18 lists the specifications for the digital output subsystem.

Table 18: DOUT Subsystem Specifications

Feature	Specifications
Number of lines	8 (Port B)
Termination	22 kΩ resistor
Outputs Output driver: Output driver high voltage: Output driver low voltage:	 74HCT244 (TTL) 2.4 V minimum (IOH = -1 mA) 0.5 V maximum (IOL = 12 mA)
Back EMF diodes	Yes

Table 19 lists the specifications for the C/T subsystems.

Table 19: C/T Subsystem Specifications

Feature	Specifications
Number of counter/timer channels	2
Clock Inputs Input type: High-level input voltage: Low-level input voltage: Minimum pulse width: Maximum frequency:	 HCT with 22 kΩ pull-up resistor 2.4 V minimum 0.8 V maximum 600 ns (high); 600 ns (low) 750 kHz
Gate Inputs Input type: High-level input voltage: Low-level input voltage: Minimum pulse width:	 HCT with 22 kΩ pull-up resistor 2.4 V minimum 0.8 V maximum 600 ns (high); 600 ns (low)
Counter Outputs Output driver high voltage: Output driver low voltage:	 3.0 V minimum @ 1 mA Source 0.4 V maximum @ 2 mA Sink

A

Table 20 lists the power, physical, and environmental specifications for the DT9800 Series function modules.

Table 20: Power, Physical, and Environmental Specifications

Feature	Specifications
Power	
+5 V Standby:	0.5 µA maximum
+5 V Enumeration:	100 mA maximum
+5 V Power ON:	500 mA maximum
+5 V Isolated Power Out (TB27)	10 mA maximum
Physical	
Dimensions:	6.5 inches x 4.5 inches x 1.4 inches
Weight:	9 ounces (255 grams)
Environmental	
Operating temperature range:	0° C to 55° C
Storage temperature range:	–25° C to 85° C
Relative humidity:	To 95%, noncondensing

Table 21 lists the screw terminal and cable specifications for the DT9800 Standard and DT9800-MAC Series function modules.

Table 21: DT9800 Standard and DT9800-MAC Series Cable and Terminal Block Specifications

Feature	Specifications
Recommended cable	2-meter, Type A-B, USB cable Data Translation part#17394, or AMP part# 974327-1
Screw terminal block	9-position terminal block Data Translation part#17381, or PCD, Inc. part# ELVP09100

Table 22 lists the connector specifications for the DT9800-EC and DT9800-EC-I Series function modules.

Table 22: DT9800-EC/EC-I Connector Specifications

Feature	Specifications
2, 26-pin locking connectors	3-M type (part number 3429)
50 pin connector	3M type; part number 3425-7000

Connector Pin Assignments

Table 23 lists the pin assignments of connector J1 on the DT9800 Standard and DT9800-MAC Series function modules.

Table 23: Pin Assignments for Connector J1 on the DT9800 Standard and DT9800-MAC Series Function Modules

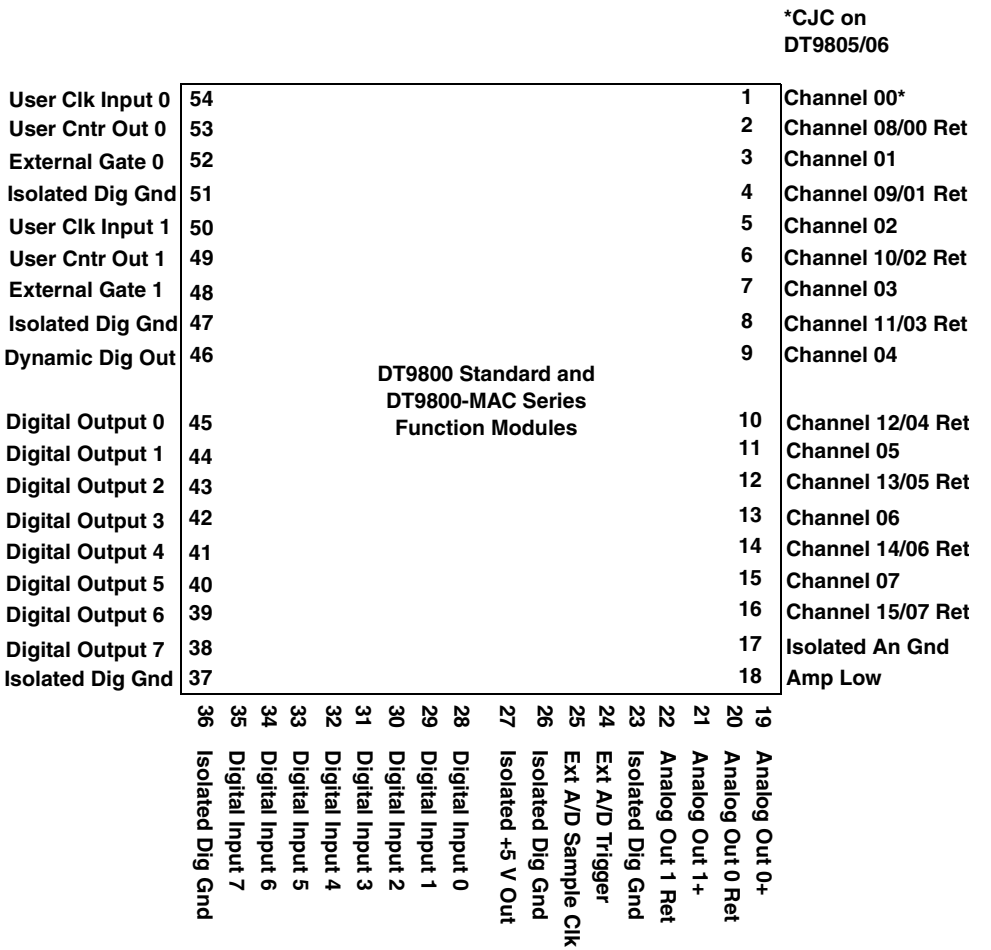
Pin Number	Signal Description	Pin Number	Signal Description
1	Analog Input 00/ CJC on DT9805/DT9806	2	Analog Input 08/00 Return
3	Analog Input 01	4	Analog Input 09/01 Return
5	Analog Input 02	6	Analog Input 10/02 Return
7	Analog Input 03	8	Analog Input 11/03 Return
9	Analog Input 04	10	Analog Input 12/04 Return
11	Analog Input 05	12	Analog Input 13/05 Return
13	Analog Input 06	14	Analog Input 14/06 Return
15	Analog Input 07	16	Analog Input 15/07 Return
17	Isolated Analog Ground	18	Amp Low
19	Analog Output 0+	20	Analog Output 0 Return
21	Analog Output 1+	22	Analog Output 1 Return
23	Isolated Digital Ground	24	External A/D Trigger
25	External A/D Sample Clock In	26	Isolated Digital Ground
27	Isolated +5 V Out[a]	28	Digital Input 0
29	Digital Input 1	30	Digital Input 2
31	Digital Input 3	32	Digital Input 4
33	Digital Input 5	34	Digital Input 6
35	Digital Input 7	36	Isolated Digital Ground
37	Isolated Digital Ground	38	Digital Output 7

Table 23: Pin Assignments for Connector J1 on the DT9800 Standard and DT9800-MAC Series Function Modules (cont.)

Pin Number	Signal Description	Pin Number	Signal Description
39	Digital Output 6	40	Digital Output 5
41	Digital Output 4	42	Digital Output 3
43	Digital Output 2	44	Digital Output 1
45	Digital Output 0	46	Dynamic Digital Output
47	Isolated Digital Ground	48	External Gate 1
49	User Counter Output 1	50	User Clock Input 1
51	Isolated Digital Ground	52	External Gate 0
53	User Counter Output 0	54	User Clock Input 0

a. +5 V output is available only when one of the subsystems is activated, which, in turn, activates power to the module.

Figure 16 shows the screw terminal assignments of the DT9800 Standard and DT9800-MAC Series function modules.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12 Channel 13/05 Ret
13 Channel 06
14 Channel 14/06 Ret
15 Channel 07
16 Channel 15/07 Ret
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18 Amp Low
36 Isolated Dig Gnd
35 Digital Input 7
34 Digital Input 6
33 Digital Input 5
32 Digital Input 4
31 Digital Input 3
30 Digital Input 2
29 Digital Input 1
28 Digital Input 0
27 Isolated +5 V Out
26 Isolated Dig Gnd
25 Ext A/D Sample Clk
24 Ext A/D Trigger
23 Isolated Dig Gnd
22 Analog Out 1 Ret
21 Analog Out 1+
20 Analog Out 0 Ret
19 Analog Out 0+

Figure 16: Screw Terminal Assignments for the DT9800 Standard and DT9800-MAC Series Function Modules

Table 24 lists the pin assignments for connector J6; Table 25 lists the pin assignments for connector J5; and Table 26 lists the pin assignments for connector J4 on the DT9800-EC and DT9800-EC-I Series function modules.

Table 24: Connector J6 Pin Assignments

J6 Pin #[a]	AC1324 Screw Terminal[a]	Signal Name	J6 Pin #[a]	AC1324 Screw Terminal [a]	Signal Name
1	TB1	Analog Input 0	2	TB2	Analog Input 0 Return/ Analog Input 8
3	TB3	Isolated Analog Ground[b]	4	TB4	Analog Input 1 Return/ Analog Input 9
5	TB5	Analog Input 1	6	TB6	Isolated Analog Ground[b]
7	TB7	Analog Input 2	8	TB8	Analog Input 2 Return/ Analog Input 10
9	TB9	Isolated Analog Ground[b]	10	TB10	Analog Input 3 Return/ Analog Input 11
11	TB11	Analog Input 3	12	TB12	Isolated Analog Ground[b]
13	TB13	Analog Input 4	14	TB14	Analog Input 4 Return/ Analog Input 12
15	TB15	Isolated Analog Ground[b]	16	TB16	Analog Input 5 Return/ Analog Input 13
17	TB17	Analog Input 5	18	TB18	Isolated Analog Ground[b]
19	TB19	Analog Input 6	20	TB20	Analog Input 6 Return/ Analog Input 14

Table 24: Connector J6 Pin Assignments (cont.)

J6 Pin #[a]	AC1324 Screw Terminal[a]	Signal Name	J6 Pin #[a]	AC1324 Screw Terminal [a]	Signal Name
21	TB21	Not Connected	22	TB22	Analog Input 7 Return/ Analog Input 15
23	TB23	Analog Input 7	24	TB24	Isolated Analog Ground[b]
25	TB25	Amp Low	26	TB26	External A/D Trigger

a. Analog input signals 8 to 15 are not available on the 5B08 or 7BP08-1 backplane. Analog input signals 4 to 15 are not available on the 7BP04-1 backplane.
b. This signal is not isolated on the DT9800-EC Series boards.

Table 25: Connector J5 Pin Assignments

J5 Pin #	AC1324 Screw Terminal	Signal Name	J5 Pin #	AC1324 Screw Terminal	Signal Name
1	TB1	Analog Output 0	2	TB2	Analog Output 0 Return
3	TB3	Analog Output 1	4	TB4	Analog Output 1 Return
5	TB5	Isolated Digital Ground[a]	6	TB6	External A/D Trigger
7	TB7	External A/D Sample Clock	8	TB8	Isolated Digital Ground[a]
9	TB9	Isolated +5 V Output[a,b]	10	TB10	Not Connected
11	TB11	Not Connected	12	TB12	Dynamic Digital Output

Table 25: Connector J5 Pin Assignments (cont.)

J5 Pin #	AC1324 Screw Terminal	Signal Name	J5 Pin #	AC1324 Screw Terminal	Signal Name
13	TB13	Isolated Digital Ground[a]	14	TB14	User External Gate 1
15	TB15	User Counter Output 1	16	TB16	User Clock Input 1
17	TB17	Isolated Digital Ground[a]	18	TB18	User External Gate 0
19	TB19	User Counter Output 0	20	TB20	User Clock Input 0
21	TB21	Not Connected	22	TB22	Not Connected
23	TB23	Not Connected	24	TB24	Not Connected
25	TB25	Not Connected	26	TB26	Not Connected

a. This signal is not isolated on the DT9800-EC Series.

b. +5 V output is available only when one of the subsystems is activated, which, in turn, activates power to the module. This signal can be used as an input to power the digital output latch so that the outputs retain their states during power down.

Table 26: Connector J4 Pin Assignments

J4 Pin #	STP-EZ Screw Terminal	Signal Name	J4 Pin #	STP-EZ Screw Terminal	Signal Name
1	TB1	Not Connected	2	TB2	Digital Ground
3	TB3	Not Connected	4	TB4	Digital Ground
5	TB5	Not Connected	6	TB6	Digital Ground
7	TB7	Not Connected	8	TB8	Digital Ground
9	TB9	Not Connected	10	TB10	Digital Ground

Table 26: Connector J4 Pin Assignments (cont.)

J4 Pin #	STP-EZ Screw Terminal	Signal Name	J4 Pin #	STP-EZ Screw Terminal	Signal Name
11	TB11	Not Connected	12	TB12	Digital Ground
13	TB13	Not Connected	14	TB14	Digital Ground
15	TB15	Not Connected	16	TB16	Digital Ground
17	TB17	Digital Output 7	18	TB18	Digital Ground
19	TB19	Digital Output 6	20	TB20	Digital Ground
21	TB21	Digital Output 5	22	TB22	Digital Ground
23	TB23	Digital Output 4	24	TB24	Digital Ground
25	TB25	Digital Output 3	26	TB26	Digital Ground
27	TB27	Digital Output 2	28	TB28	Not Connected
29	TB29	Digital Output 1	30	TB30	Not Connected
31	TB31	Digital Output 0	32	TB32	Not Connected
33	TB33	Digital Input 7	34	TB34	Not Connected
35	TB35	Digital Input 6	36	TB36	Not Connected
37	TB37	Digital Input 5	38	TB38	Not Connected
39	TB39	Digital Input 4	40	TB40	Not Connected
41	TB41	Digital Input 3	42	TB42	Not Connected
43	TB43	Digital Input 2	44	TB44	Not Connected
45	TB45	Digital Input 1	46	TB46	Not Connected
47	TB47	Digital Input 0	48	TB48	Not Connected
49	TB49	Not Connected	50	TB50	Not Connected

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